

A SINGLE INDUCTOR, MULTIPLE INPUT PIEZOELECTRIC INTERFACE
CIRCUIT CAPABLE OF HARVESTING ENERGY FROM ASYNCHRONOUSLY
VIBRATING SOURCES

A Thesis

by

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ABSTRACT

The energy harvesting industry has seen steady growth in recent years. This growth has been driven by the increasing demand for remote sensing, implantable technologies, and increased battery life in mobile and hand held devices. Due to the limited amount of energy available from ambient sources, any system that attempts to harness energy from them should necessarily be highly efficient to make the net output power useful.

A lot of work has been done on minimizing losses in piezoelectric energy harvesters. Most of this has however been limited to harvesters with single vibration sources or multiple sources vibrating synchronously. This work presents a multiple input piezoelectric energy harvester capable of harvesting from multiple piezoelectric energy sources vibrating asynchronously (at different frequencies, or at the same frequency but in different phases) using a single inductor. The use of a single inductor eliminates the extra quiescent power consumption, component count, printed circuit board real estate that would have been incurred by using a one inductor per input device.

The inductor is time shared between three input devices using a digital control circuit which regulate access to the inductor while avoiding any destructive interaction between the input devices. The chip was designed in a $0.18\mu\text{m}$ technology and achieves a conversion efficiency of 60%. Testing with three asynchronously vibrating sources shows that the chip extracts maximum power from all inputs simultaneously, independent of vibration frequency or phase.

ACKNOWLEDGEMENTS

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I offer this preemptive apology recognizing that I most probably have missed some names. In typical student fashion, I am writing this thesis a bit behind schedule and I am pulling all nighters on end to make sure I meet the deadline. Do not mistake my forgetfulness for lack of appreciation. I am immensely grateful to you all.

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1. INTRODUCTION

The proliferation of wireless portable and hand held electronic devices has brought along with it the need for low power design techniques and efficient power management. While these devices create avenues for exciting applications like building monitoring, environmental control, and wireless sensor networks for the Internet of Things(IOT), they provide a unique low power design challenge. Reducing power consumption goes a long way to increasing battery life, mostly by reducing the frequency of battery recharge. Within the limits of performance requirements however, further battery life extension only becomes possible through the provision of alternative energy sources. Recent advances in low power VLSI circuit design has seen the reduction in power consumption for many wireless applications to the range of tens to hundreds of microwatts [3]. This is especially possible in applications where the devices are required to be active for short widely spaced intervals. Such low power levels makes these devices amenable to self-sustainability, especially in remote applications where battery replacement is impractical. Due to the very low power requirements, the use of energy scavengers for such applications becomes a very feasible possibility. This chapter examines the available ambient energy sources as well as the development of energy harvesting technologies for each of the sources over the years.

1.1 Energy Harvesting Technologies

CMOS technologies have scaled down over the years according to Moore's Law. Along with this scaling comes a reduction in device power supplies and therefore power consumption. This has led to the development of high density integrated circuits with increased functionality and reduced power consumption, creating the

potential for the miniaturization of devices with extremely high functionality. Many mobile and wireless applications have developed as a result. Battery technology has, however, not kept up with the power requirements of these applications [1]. They have lagged behind in density, reliability and lifetime, with the state of the art energy density only about 10X its value 24 years ago, as can be seen in Figure 1.1. The floor plan for a typical sensor module for remote monitoring is shown

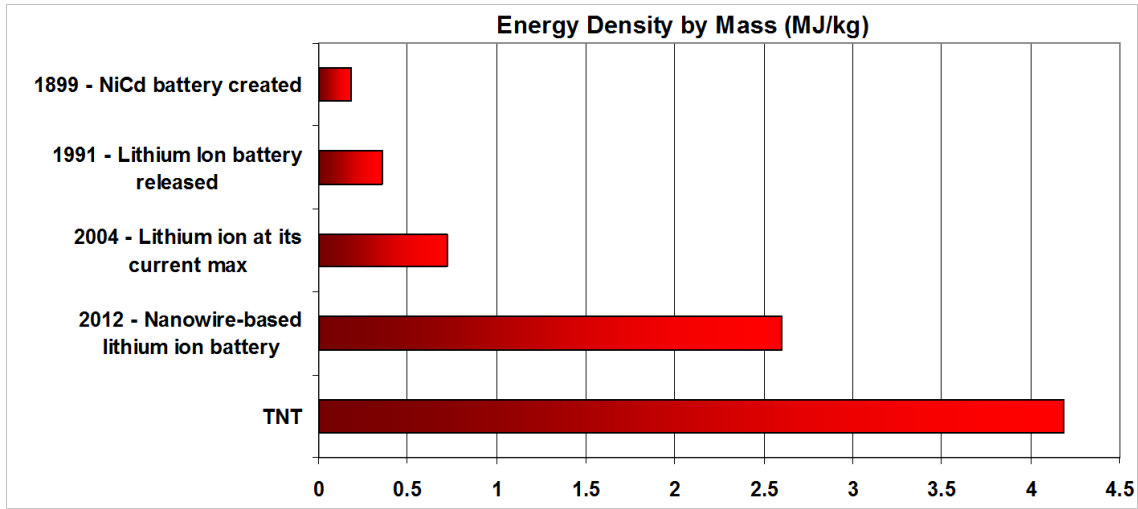


Figure 1.1: Battery energy density over the years [1]

in Figure 1.2. In applications where these nodes are deployed in locations that are not easily accessible, frequent battery replacement becomes impractical. These factors along with the abundance of ambient energy sources make energy harvesting a viable alternative to batteries and fuel cells as power sources for mobile and wireless networks. A lot of possible sources of ambient energy have been identified over the many years of research into energy harvesting. An objective parameter for evaluating ambient energy sources is power density. This is simply defined as the average power

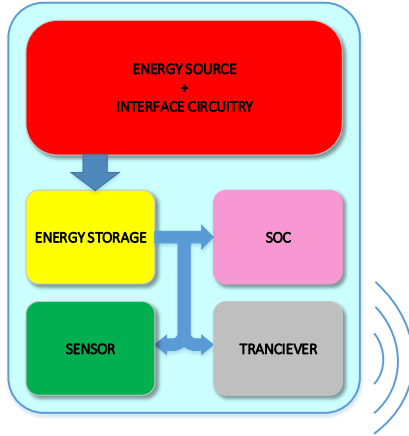


Figure 1.2: Floor plan of a typical IOT sensor module

harvested per cm^3 of energy harvesting material. Table 1.1 shows a broad survey of energy harvesting sources and their respective power densities. The table shows a

Table 1.1: Survey of power scavenging and ambient energy sources [3]

| | Power density one year lifetime ($\mu W/cm^3$) | Power density 10 year lifetime($\mu W/cm^3$) |
|-------------------------------------|--|--|
| Solar(outdoors) | 15,000-Direct sun 150 - Cloudy day | 15,000-Direct sun 150 - Cloudy day |
| Solar(indoors) | 6-Office desk | 6-Office desk |
| Vibrations(piezoelectric) | 250 | 250 |
| Vibrations(electromagnetic) | 50 | 50 |
| Acoustic Noise | 0.003 @ 75dB 0.96 @ 100dB | 0.003 @ 75dB 0.96 @ 100dB |
| Temperature gradient | 15 @ 10°C gradient | 15 @ 10°C gradient |
| Shoe Inserts | 330 | 330 |
| Batteries(non-rechargeable lithium) | 45 | 3.5 |
| Batteries(rechargeable lithium) | 7 | 0 |
| Hydrocarbon fuel(microheat engine) | 333 | 33 |
| Fuel cells(methanol) | 280 | 28 |

the clear superiority of energy harvesting sources over fixed power sources (batteries) in terms of long term reliability. Batteries provide a very reliable source of energy over the short term and are therefore suitable for devices where the battery is readily accessible and as such easily replaceable. An application like wireless pressure sensing in oil wells, however require a long term reliability that batteries cannot provide. Solar energy has the highest power density ($15000\mu W/cm^3$) and is the most widely used source of ambient energy. In applications that have minimum exposure to sunlight, however vibration becomes a more viable candidate. The sources can also be combined to obtain maximum power across different environmental conditions, although such a system will require some additional power management circuitry.

1.2 Ambient Energy Sources

1.2.1 Solar Energy

Solar energy has been an alternative source of energy for a considerable amount of time and the development of efficient photovoltaic cells has been an attractive area of research for many years. To this end, solar energy leads the pack by quite some distance in terms of power density as can be seen in Table 1.1. The schematic of a generic solar cell is shown in Figure 1.3. It consists of a PN junction, which generates a voltage across its terminals when a photon passes through it. Silicon solar cells are a mature technology, with efficiencies of single crystal silicon cells ranging from 12% to 25%. These can however be quite expensive, and might not be viable for large sensor networks. Thin film polycrystalline, and amorphous silicon solar cells are also commercially available and cost less than single crystal silicon, albeit with lower efficiency. The terminal impedances of a solar cell changes with different light intensities, and therefore elaborate schemes are required to sense the impedance of the cells and present a matching load to ensure maximum power transfer [14]. Many

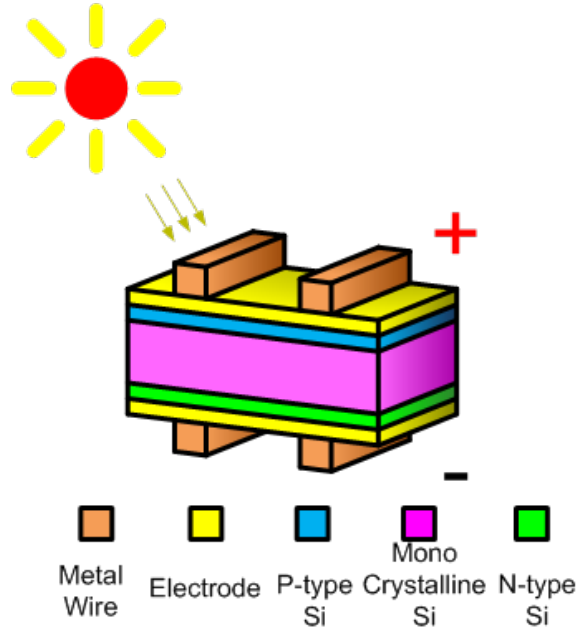


Figure 1.3: Generic solar cell

Maximum Power Point Transfer(MPPT) schemes have been developed to this end. While solar cells provide a considerable amount of energy in the presence of a direct sunlight, their output in indoor environments leave a lot to be desired. As can be seen from Table 1.1 the energy density of solar cells falls to $6\mu W/cm^3$ for an office environment from the $15mW/cm^3$ that was obtained for direct sunlight. This limits its use in applications with little exposure to direct sunlight.

1.2.2 Thermal Energy

Thermoelectric generators (TEG) offer an attractive way of harvesting thermal energy. By utilizing a temperature gradient across specific semiconductor materials, a voltage is generated which is given by the Seebeck coefficient. This coefficient is the measure of an induced thermoelectric voltage in response to temperature differences across its surfaces. Figure 1.4 shows a typical thermoelectric generator module. Any

environment which offers a temperature difference or where a temperature difference can be established potentially offers an unlimited power source through a TEG implementation. The TEGs output voltage is directly proportional to the temperature difference between its two junctions [15]. Depending on the application, there can

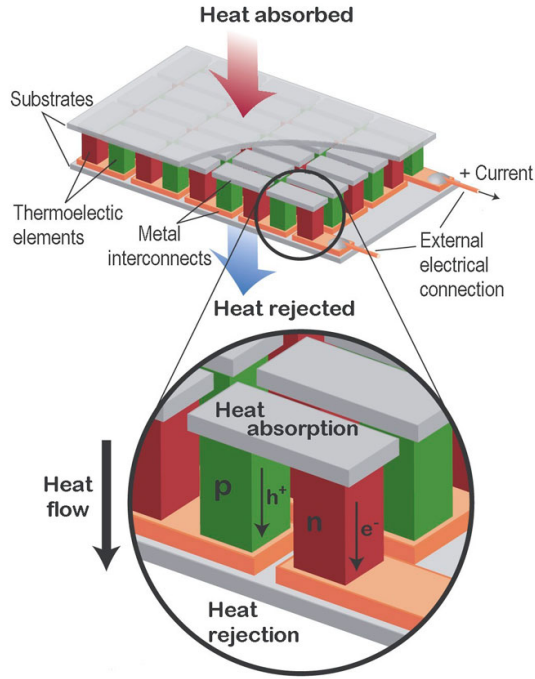


Figure 1.4: Thermoelectric generator module [2]

be as little as 0.5 to 1°C of temperature difference between the surfaces and up to 50°C under optimum conditions. For small devices ($> 10\text{mm}^2$ area) this leads limited available power. This limited power condition requires a step-up DC-DC converter in order to adequately boost the TEG output voltage levels to levels which can be utilized by CMOS process.

1.2.3 Kinetic Energy

Kinetic energy is fast becoming a very reliable alternative source of electrical energy and can achieve energy densities up to $250\mu W/cm^3$, second only to solar energy. From basic footfalls during walking to the vibrations associated with the operation of heavy duty machinery, various sources of ambient kinetic energy exist that can easily be harvested to produce electricity. Kinetic energy harvesting can be treated under three headings: Electrostatic, Electromagnetic, and Piezoelectric.

1.2.3.1 Piezoelectric Energy Harvesting

Piezoelectric materials are materials produce electrical energy in response to mechanical stress or conversely deform in the presence of an electric field. Currently, the most common piezoelectric materials are polycrystalline ceramics like Lead Ziconate Titanate (PZT) and Barium Titanate ($BaTiO_3$) which was the first piezoelectric material discovered [16]. Another example of a piezoelectric material is Polyvinylidene fluoride (PVDF), a thermoplastic fluoropolymer, which has found popular use in energy harvesting from floors due to its amorphous nature. Under excitation by an external periodic vibration, these transducers produce an AC voltage across their terminals. This suggests the need for some form of rectification and power conditioning before the energy can be supplied to a practical load. Owing to the parasitic internal capacitance of the piezoelectric devices, a matched conjugate impedance should be presented to the device in order to extract maximum power. The physics of piezoelectric devices as well as the loading requirements for maximum power transfer is treated in more detail, in the subsequent chapters. While Piezoelectric harvesters have the highest energy density of all three kinetic energy harvesting methods, their limited potential for MEMS scale integration means they cannot be readily applied in fully integrated energy harvesting solutions.

1.2.3.2 *Electrostatic Energy Harvesting*

Electrostatic energy harvesters generate power by altering the capacitance of a charged capacitor using its physical dimensions. The energy stored in a capacitor of capacitance C charged to a voltage V is given by

$$E = \frac{1}{2}CV^2 = \frac{Q^2}{2C} \quad (1.1)$$

Thus by using a mechanical structure whose capacitance can be changed through vibrations, the energy stored in the capacitor can be increased by either holding charge constant and reducing capacitance or keeping voltage constant and increasing capacitance. Either way, a potential for creating energy from vibrations exists. One major advantage of electrostatic harvesters is their potential for integration using MEMS technology. Three different types of MEMS electrostatic generators are shown in Figure 1.5. Each type vibrates in a different direction to obtain a varying capacitance. The capacitances of typical MEMS electrostatic generators vary from 50pF to 400pF [17–21]. Two basic energy harvesting modes exist for electrostatic generators: the constant charge mode and the constant voltage mode [22]. The main challenge of the constant charge mode is that the voltage across the variable capacitance can reach several hundreds of volts exceeding the breakdown voltages of most vanilla CMOS processes. The advanced technologies that can handle such voltages are typically too expensive to make this approach practical for high volume production. The constant voltage mode is therefore the approach of choice for most electrostatic harvesters. A major drawback of electrostatic harvesters is that they require an initial charge to kick start the harvesting process.

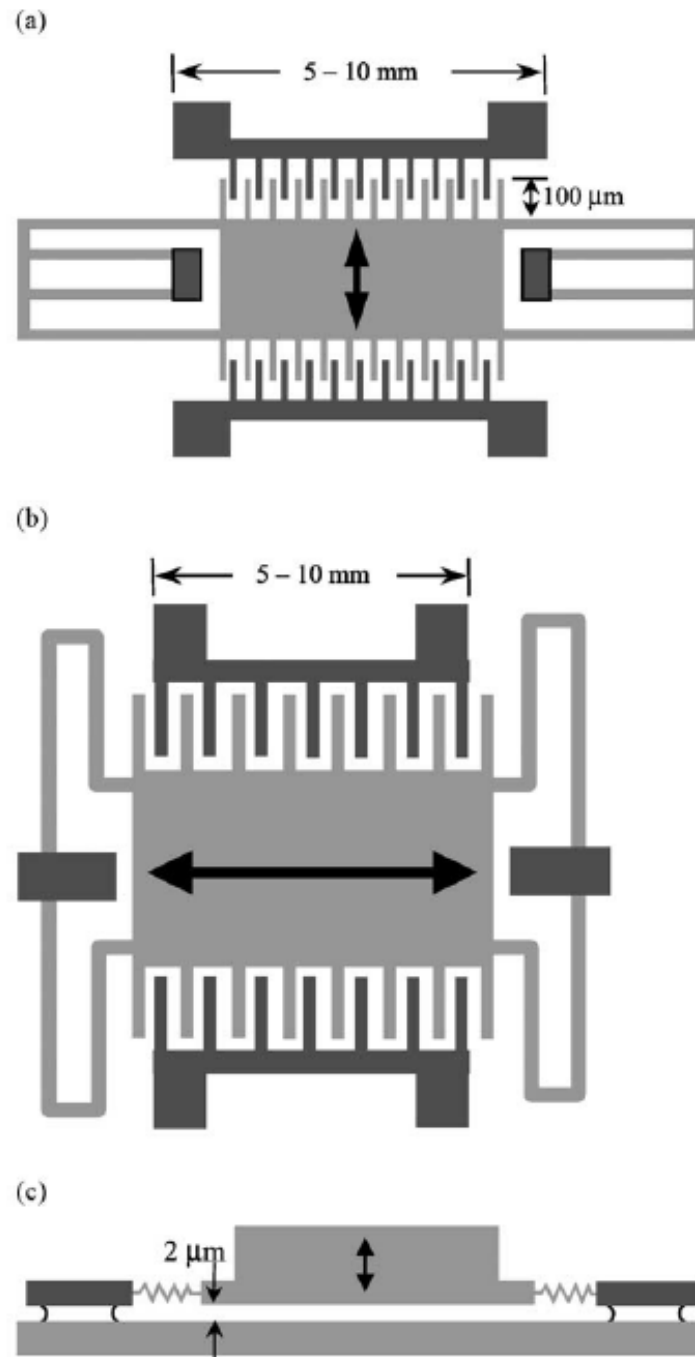


Figure 1.5: Three types of electrostatic generators (a) In-plane overlap converter (b) In-plane gap closing converter (c) Out-of-plane gap closing converter [3]

1.2.3.3 Electromagnetic Energy Harvesting

Electromagnetic or inductive energy harvesting employs the basic principle of electromagnetic induction(similar to hydro-electric generators) to produce energy. Energy is generated by creating relative motion between a conductor and a magnetic field. A typical electromagnetic energy harvester is shown in Figure 1.6. It consists

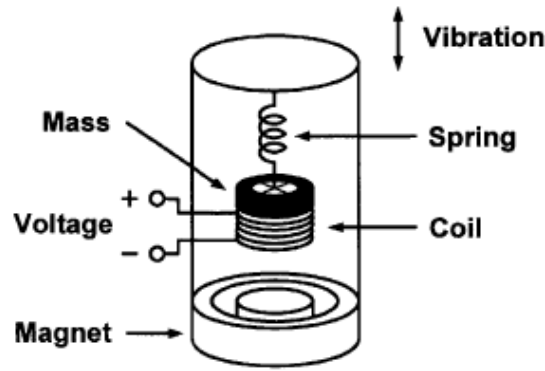


Figure 1.6: Schematic of a typical electromagnetic energy harvester ©IEEE 1998 [4]

of a coil wound around a mass which hangs from the casing of the structure by means of a spring. A permanent magnet attached to the bottom of the device provides the magnetic field. The coil moves through the magnetic field when the mass vibrates producing electrical energy in the process according to Faraday's Law. As with piezoelectric and electrostatic harvesters, electromagnetic energy harvesters, produce AC voltages that require some form of rectification to make them suitable as power sources for portable electronics. Their output voltages, however, have very low amplitudes ($< 150mV$), creating the need for converters with very low input thresholds. This can be a big design challenge especially with low cost CMOS

technologies.

1.3 Applications of Piezoelectricity

The applications of piezoelectricity can be grouped into three: energy harvesting, sensing(as a transducer) and actuation. It has the added advantage of being compact (second to electrostatic harvesters but produces more energy), making it amenable to mobile and wireless systems. One application that has gained increased popularity in recent times is the use of piezoelectric materials to harvest energy from floors [23,24]. Pavegen Systems and Energy Floors, have both developed compact robust floor tiles modules that show a lot of promise in this particular application. A demonstration at the Paris Marathon in 2009 generated up to 4.7 kWh of energy [25]. The tile module from Pavegen Systems is shown in Figure 1.7. Each tile produces up to



Figure 1.7: Pavegen Systems floor tile [5]

7W of power per step. Many kilowatts of power can be generated in areas of high pedestrian and/or vehicular traffic, which could provide a clean energy source for street lights, bill-boards, etc.. Other reported applications include energy harvesting

from the soles of shoes [6, 26, 27], and from the tensile stress generated in backpack straps [28]. The power outputs in these applications are however in the mW range, making them well suited as main (or back-up) supplies for low power electronics.

In the applications described so far, energy is produced from tensile stress due to deformation rather than vibration. Thus the more flexible PVDF (and other polymers) is the material of choice. To harvest energy from vibrating heavy duty machinery however, the more brittle ceramics (PZT, etc.) are used. Piezoelectric materials are also used for structural monitoring in bridges, interchanges and other mechanical structures. They convert the mechanical stresses within these structures to electric current which can be processed to provide an accurate measure of structural integrity. They are also used as actuators in piezoelectric speakers , and as sensors (force and pressure) in a wide variety of applications.

1.4 Research Trends

The ultimate goal of most energy harvesting research is to establish ambient energy as a staple power source for autonomous mobile systems. To this end a lot work is currently being done in reducing the form factors of most energy harvesters to make them more amenable to such systems. The integrability of MEMS (Micro-Electromechanical Systems) technologies has been leveraged in this regard. This has led to the development of fully integrated systems with both harvesters and power management circuitry integrated on the same chip [29]. While such systems have been limited to piezoelectric and electrostatic energy harvesters, the potential for further integration creates even more possibilities.

Body area networks (BAN) have generated a lot of interest in recent times. This has in turn generated even more interest in the development of the wearable sensor nodes that lie at the very core of BANs. Integration of sensors and energy harvesters

in wearables like watches, shoes and even in textiles [30] has become a popular area of research as a result. A shoe with a piezoelectric insert for energy harvesting is shown in Figure 1.8. Maintaining high efficiency in such wearables is still a major challenge and a very well researched area.

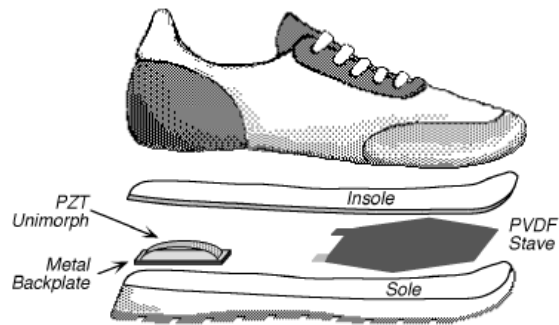


Figure 1.8: Energy harvesting from piezoelectric shoe insert ©IEEE 1998 [6]

2. PIEZOELECTRIC DEVICE PHYSICS

This chapter examines the physics of piezoelectric devices. A generic model for the conversion of vibrational energy to electrical energy is first developed and the result is applied to a piezoelectric energy harvesting system.

2.1 Conversion of Vibrational Energy to Electrical Energy

Vibration based generators can essentially be modeled as an equivalent lumped spring mass system. Using this model the general equations for energy conversion can be determined independent of the actual energy conversion mechanisms. A simple single degree of freedom model based on the model in [31] is shown in Figure 2.1

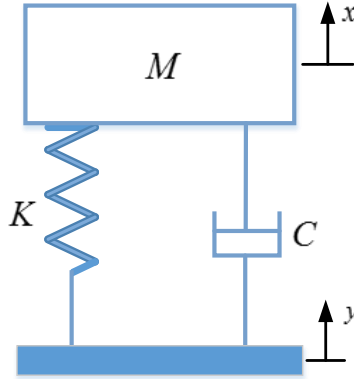


Figure 2.1: Equivalent lumped spring mass system of a vibrating rigid body

The governing equation of motion for the mass M can be written as

$$M\ddot{z} + C\dot{z} + Kz = -M\ddot{y} \quad (2.1)$$

where $z = x - y$ is the net displacement of the mass, K is the spring constant and C is the damping force which has two components: the electrically induced damping force (C_E) and the mechanical damping force C_M i.e $C = C_E + C_M$. For piezoelectric devices, these damping components are not necessarily linear in themselves, or proportional to velocity [7]. These assumptions will however be used in the forgoing analysis as they will allow for some very insightful conclusions to be drawn. Following the analysis in [7], the mechanical energy converted to electrical energy is equal to the work done against the mechanical restoring force by the electrically induced damping. The electrically induced damping force F_E is simply $C_E \dot{z}$. The electrical power generated is therefor given by

$$P = \int_0^v F_E dv \quad (2.2)$$

where $v = \dot{z}$ is the velocity of the vibrating mass. Substituting $F_E = C_E v$ into equation 2.2 yields

$$P = C_E \int_0^v v dv \quad (2.3)$$

$$= \frac{1}{2} C_E v^2 = \frac{1}{2} C_E \dot{z}^2 \quad (2.4)$$

The complete expression for power can be obtained by solving equation 2.1 for \dot{z} and substituting the result into 2.4. Taking the Laplace transform of equation 2.1 and solving for $Z(s)$ we have

$$Z(s) = \frac{-Ms^2 Y(s)}{Ms^2 + Cs + K} \quad (2.5)$$

where $Z(s)$ and $Y(s)$ are the Laplace transforms of the displacement of the mass and the input displacement respectively. Using the conventional notation for a second

order system, we have,

$$Z(s) = \frac{-s^2 Y(s)}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad (2.6)$$

where

$$\omega_n = \sqrt{\frac{K}{M}} \quad (2.7)$$

and

$$\zeta = \frac{C}{2\sqrt{MK}} = \frac{C_M}{2\sqrt{MK}} + \frac{C_E}{2\sqrt{MK}} = \zeta_E + \zeta_M \quad (2.8)$$

Using $s = j\omega$, recalling that $\mathcal{L}\{\dot{z}\} = sZ(s)$, taking the absolute value of both sides of the equation 2.6 and re-arranging, we have,

$$|\dot{Z}| = \left| \frac{j\omega \left(\frac{\omega}{\omega_n}\right)^2}{1 - \left(\frac{\omega}{\omega_n}\right)^2 + j2\zeta \left(\frac{\omega}{\omega_n}\right)} \right| |Y| \quad (2.9)$$

From which

$$|\dot{Z}|^2 = \frac{\omega^2 \left(\frac{\omega}{\omega_n}\right)^4}{\left[2\zeta \left(\frac{\omega}{\omega_n}\right)\right]^2 + \left[1 - \left(\frac{\omega}{\omega_n}\right)^2\right]^2} |Y|^2 \quad (2.10)$$

Now from equation 2.8,

$$C_E = 2\zeta_E \sqrt{MK} = 2\zeta_E M\omega_n \quad (2.11)$$

Substituting 2.11 and 2.10 into 2.4 yields the following result

$$P = \frac{M\zeta_E Y^2 \left(\frac{\omega}{\omega_n}\right)^3 \omega^3}{\left[2\zeta \left(\frac{\omega}{\omega_n}\right)\right]^2 + \left[1 - \left(\frac{\omega}{\omega_n}\right)^2\right]^2} \quad (2.12)$$

This is the expression for the electrical output power from a generalized vibration based energy harvester vibrating at a frequency ω . It is quite straight forward to show that the power reaches its maximum when $\omega = \omega_n$ (this is obtained from the solution of $\frac{\partial P}{\partial \omega} = 0$). Setting $\omega = \omega_{max} = \omega_n$ and solving for P yields the following expression for the maximum power

$$P_{max} = \frac{MY^2\omega_n^3\zeta_E}{4\zeta^2} \quad (2.13)$$

A plot of normalized power versus frequency is shown in Figure 2.2 for different values of ζ . This illustrates the frequency selectivity of vibration based energy harvesters.

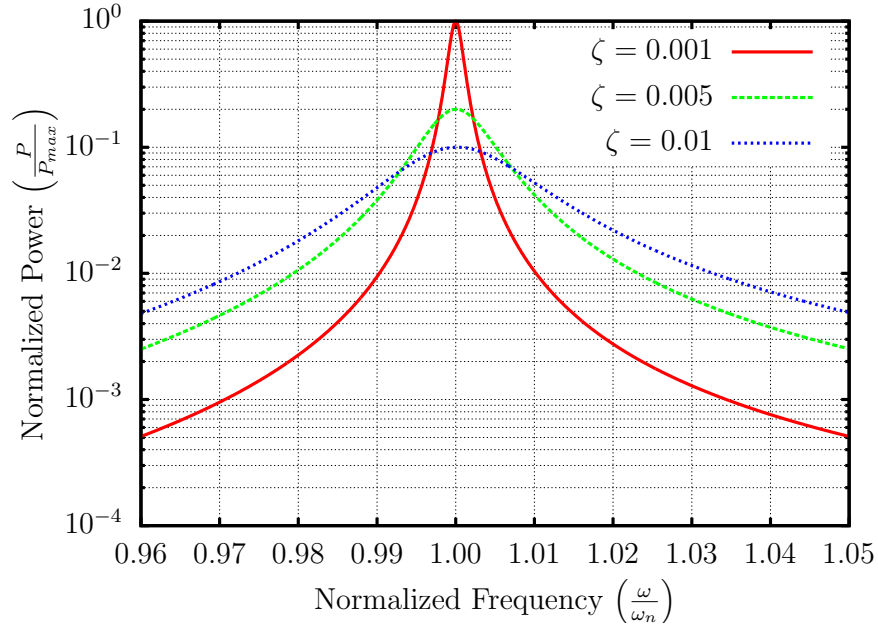


Figure 2.2: Power spectrum of generic vibration based energy harvester [7]

A direct trade-off exists between maximum power and bandwidth of operation as can be seen from Figure 2.2. Low ζ reduces the bandwidth of operation but increases

the maximum power and vice versa. The most appropriate value of ζ depends on the particular application. Although low damping ratio systems, provide higher values of P_{max} , their output power drops significantly with the slightest deviation from the resonant frequency. Such devices will therefore be unsuitable for systems in which the frequency of vibration varies across a wide range.

As was done for equation 2.14, one can easily show that P_{max} reaches its maximum when $\zeta_E = \zeta_M$. The results from the analysis above can be summarized into the following conclusions:

- For fixed values of ζ_E and ζ_M maximum power is extracted around the resonant frequency of the piezoelectric device.
- The maximum power of a piezoelectric device vibrating at its resonant frequency is maximized when $\zeta_E = \zeta_M$

A plot of the normalized maximum power against the electrical damping factor is shown in Figure 2.3 for three different values of ζ_M . It can be seen from the graph that for each value of ζ_M , P_{max} reaches its maximum when $\zeta_E = \zeta_M$. Another very important deduction from the graph is that the maximum value of P_{max} is higher for lower values of ζ_M . Low values of ζ_M however reduce the useful bandwidth of the device, limiting its application to vibrations with low bandwidths. The output power can also be increased by increasing the vibrating mass. While this also indirectly reduces the damping factor and hence the bandwidth of operation, the linear term in the numerator of the power expression ensures that the power output increases much faster than the bandwidth reduces.

Two general methods of handling the trade-off between peak output power and bandwidth have been reported in the literature: using low bandwidth devices with tunable resonance frequencies and increasing the bandwidth of the devices without

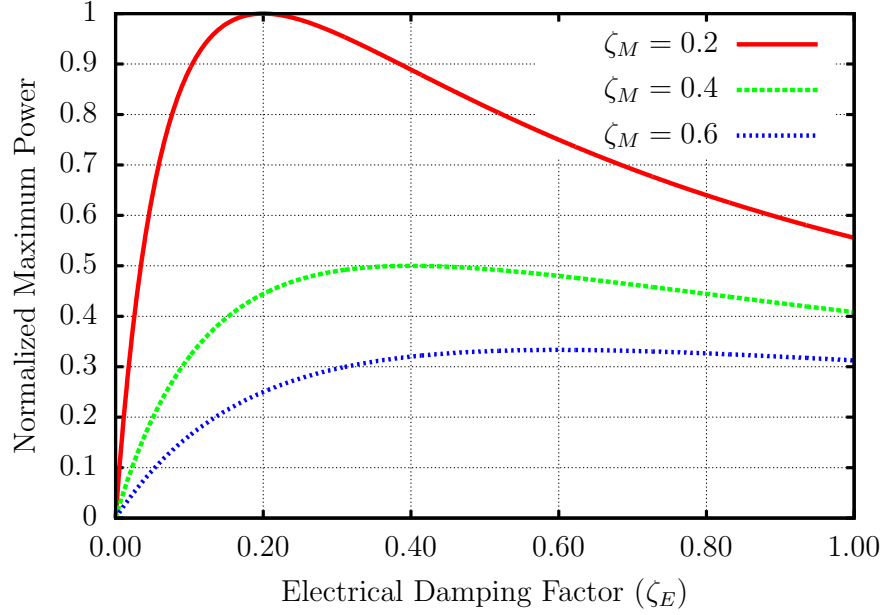


Figure 2.3: Normalized maximum power vs electrical damping

sacrificing power. Both approaches are extensively treated in the literature in a number of implementations, each with its own merits and niche.

2.2 Piezoelectric Device Modeling

This section examines piezoelectric devices in more detail, formulating the electromechanical energy conversion equations. A compact circuit model is then developed which is used in subsequent chapters for circuit simulations. The schematic of a typical piezoelectric bimorph with an attached proof mass is shown in Figure 2.4. The constitutive equations for the piezoelectric bimorph can be written as [32]

$$\delta = \frac{\sigma}{Y} + dE \quad (2.14)$$

$$D = \varepsilon E + d\sigma \quad (2.15)$$

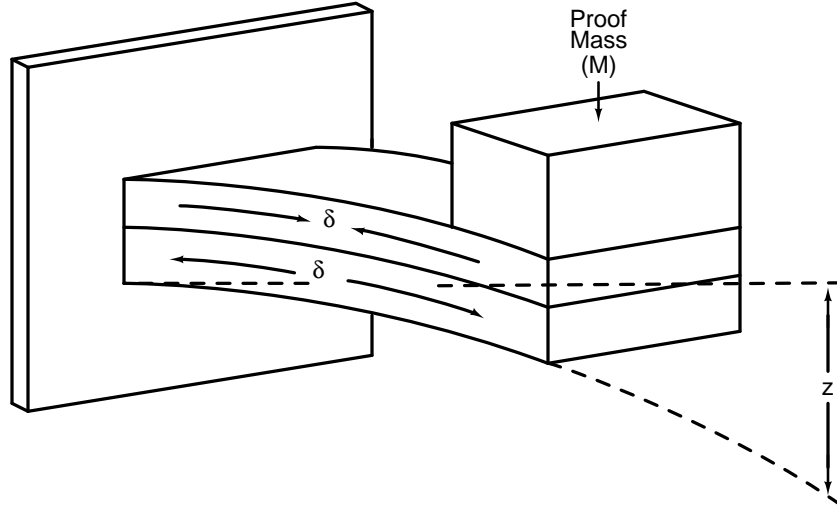


Figure 2.4: Piezoelectric bimorph with a proof mass

where

δ – Mechanical Strain

d – Piezoelectric strain coefficient

σ – Mechanical Stress

E – Electric Field

Y – Young’s Modulus

D – Electric Displacement

ϵ – Dielectric Constant

Two main equivalent models have been developed from the above equations: the spring mass damper model and the transformer based circuit model. Both are briefly presented in the following sections.

2.2.1 Spring Mass Damper Model

The most common model used is the spring mass damper model [33]. This can easily be obtained from the constitutive equations by re-writing them in terms of the relevant macro-variables i.e. Force(F), Displacement (u), Voltage (V), and Current (I). The resulting model is shown in Figure 2.5. The effect of the piezoelectric

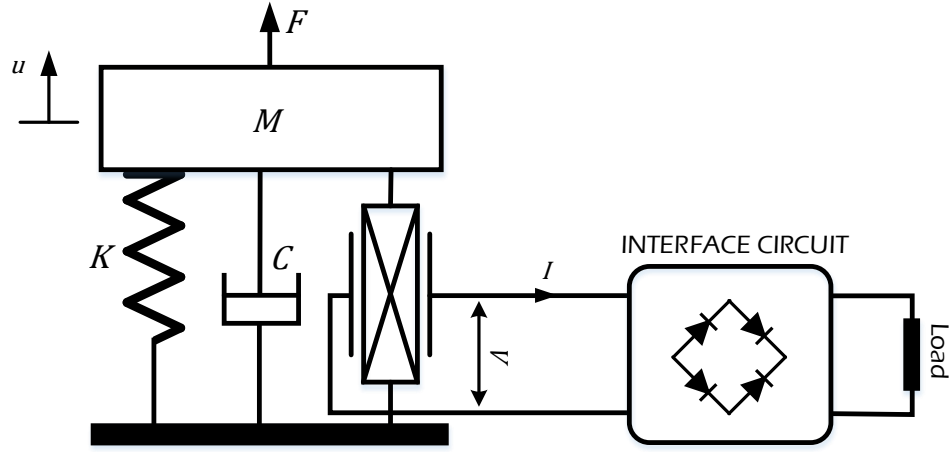


Figure 2.5: Equivalent spring mass damper model of a piezoelectric energy harvester

disk is to generate a voltage dependent force that adds to the restoring force of the spring mass system. If all transduction losses are neglected, the work done by this component is equal to the electrical energy generated by the disk. The force F represents the mechanical excitation applied to the structure. The piezoelectric equations relate the mechanical variables of the device (u, F_P) to the electrical variables (I, V) as follows [33]

$$F_P = K_{PE}u + \alpha V \quad (2.16)$$

$$I = \alpha \dot{u} - C_p \dot{V} \quad (2.17)$$

The expressions for K_{PE} , C_p , and α are given in equations 2.18 as a function of the parameters defined in Table 2.1

$$K_{PE} = \frac{YA}{L}, \quad C_p = \frac{\varepsilon A}{L}, \quad \alpha = \frac{eA}{L} \quad (2.18)$$

To allow for electrical simulation of the model, a circuit model is developed by using

Table 2.1: Piezoelectric parameters

| Parameter | Definition |
|---------------|---|
| A | Piezoelectric disk cross sectional area |
| L | Piezoelectric disk thickness |
| Y | Young's Modulus of short circuited piezoelectric disk |
| ε | Clamped permittivity of piezoelectric disk |
| α | Piezoelectric coefficient of piezoelectric disk |

a standard RLC circuit to model the mechanical portion using and a transformer for electromechanical coupling. This leads to a model containing only primitive SPICE elements that can be used in circuit simulation. The model is developed in more detail in the next section.

2.2.2 Transformer Based Circuit Model

In this model, the mechanical portion of the spring mass damper model is realized using an RLC circuit. The electromechanical transduction mechanism is modeled

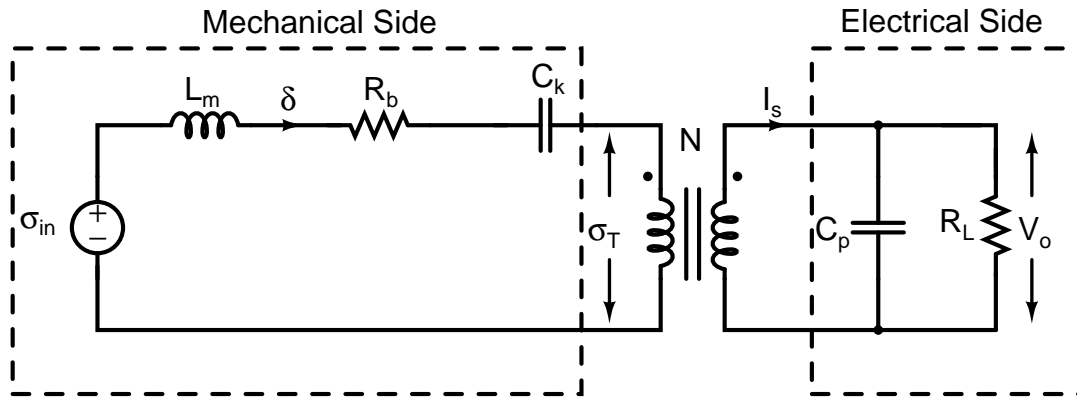


Figure 2.6: Transformer circuit model for piezoelectric bimorph

using a transformer providing a compact circuit model that can be used in SPICE simulations as shown in Figure 2.6. The model is briefly formulated in this section following the procedure described in [32]. The mechanical portion modeled on the primary side of the transformer where the mechanical strain "flowing" through the elements generates mechanical stress across them. The secondary models the electrical portion of the device and therefore has current and voltage as state variables. A detailed derivation of all parameters is presented in [32]

The transformer models the electromechanical transduction mechanism. The turns ratio will relate

- Strain across its primary terminal to electric field (voltage) on the secondary under no load (zero electrical displacement).
- Electric displacement in the secondary to stress in the primary under zero electric field secondary short circuited)

Solving the constitutive equations under these conditions yields

$$\sigma = -dYE \tag{2.19}$$

$$D = dY\delta \tag{2.20}$$

From 2.21 and 2.22, we can deduce than the equivalent turns ratio $N = dY$. This turns ratio relates strain (σ) and stress (δ) in the primary to electric field and electric displacement in the secondary. Since the state variables used in the secondary are voltage and current, further modifications are necessary. Using $D = \frac{q}{awl_e}$ and $V = \frac{Et_c}{a}$ ($a = 1$ for parallel connection and $a = 2$ for series connection) and recalling that

$I = \dot{q}$ we have

$$I_s = \dot{q} = awl_e dY \dot{\delta} \quad (2.21)$$

$$\sigma_T = \left(\frac{adY}{2t_c} \right) V_T \quad (2.22)$$

From the above expressions we obtain the transformer voltage transformation ratio $N = \frac{adY}{2t_c}$ and the current transformation ratio $A_i = awl_e dY$. It very important to note that the transformer used in the model is not a real transformer in the electrical sense as the voltage transformation ratio is not equal to the reciprocal of the current transformation ratio [34]. Typical impedance transformation methods for transformers are therefore not applicable. The fictitious transformer however allows for a compact modeling of the electromechanical coupling mechanism. Applying KVL on the mechanical side of the transformer, we have

$$\sigma_{in} = \sigma_L + \sigma_R + \sigma_C + \sigma_T \quad (2.23)$$

It can be shown (see [32] for details) that

$$\sigma_L = \frac{m}{b^* b^{**}} \ddot{\delta}; \quad \sigma_R = \frac{b_m}{b^*} \dot{\delta}; \quad \sigma_C = Y_c \delta; \quad \sigma_{in} = \frac{m}{b^{**}} \ddot{y} \quad (2.24)$$

where b_m is the damping coefficient, Y_c is the elastic constant (Young's modulus) of the short circuited disk, \ddot{y} is the acceleration of the input vibration and b^* and b^{**} are defined as follows [32]

$$b^{**} = \frac{2I}{b(2l_b + l_m - l_e)} \quad (2.25)$$

$$b^* = \frac{3b}{l_b^2} \frac{(2l_b + l_m - l_e)}{(2l_b + \frac{3}{2}l_m)} \quad (2.26)$$

where I is the moment of inertia of the disk and b, l_m, l_b and l_e are physical dimensions of the disk (see [32] for details). Substituting 2.24 into 2.23 yields the following equation which describes the mechanical dynamics of the system in the presence of electrical coupling

$$\ddot{\delta} = -\frac{Yb^*b^{**}}{m}\delta - \frac{b_mb^{**}}{m}\dot{\delta} + \frac{adY_c}{2t_c}\frac{b^*b^{**}}{m}V_o + b^*\ddot{y} \quad (2.27)$$

Applying KCL to the secondary yields the following equation for the electrical portion of the model [32]

$$\dot{V}_o = -\frac{2Y_c dt_c}{a\varepsilon}\dot{\delta} - \frac{1}{R_L C_P}V_o \quad (2.28)$$

Taking the Laplace transforms of 2.27 and 2.28 yields the following equations

$$\Delta(s) \left(s^2 + \frac{b_mb^{**}}{m}s + \frac{k_{sp}}{m} \right) = \frac{adk_{sp}}{2mt_c}V_o(s) + b^*A_{in}(s) \quad (2.29)$$

$$\Delta(s) = -\frac{a\varepsilon}{2Y_c dt_c s} \left(s + \frac{1}{R_L C_P} \right) \quad (2.30)$$

where $\Delta(s)$ is the Laplace transform of the mechanical stress, $k_{sp} = Yb^*b^{**}$ is the effective elastic constant and $A_{in} = \ddot{y}$ is the input acceleration. The coefficients of the on the left hand side of 2.29 can be written in terms of standard second order system variables. Substituting $\omega_n = \frac{k_{sp}}{m}$, $\zeta = \frac{b_mb^{**}}{2k_{sp}}$, $s = j\omega$ and eliminating $\Delta(s)$ from 2.29 and 2.30 yields the following transfer function [32]

$$\frac{V_o(\omega)}{A_{in}(\omega)} = \frac{-j\omega \frac{2Y_c dt_c b^*}{a\varepsilon}}{\frac{\omega_n^2}{R_L C_P} - \left(\frac{1}{R_L C_P} + 2\zeta\omega_n \right) \omega^2 + j\omega \left[\omega_n^2(1 + k^2) + \frac{2\zeta\omega_n^2}{R_L C_P} - \omega^2 \right]} \quad (2.31)$$

where $k = \sqrt{d^2 Y_c / \varepsilon}$, is the piezoelectric coupling coefficient. When the excitation

frequency becomes equal to the natural frequency of the disk ω_n , 2.31 reduces to [32]

$$\frac{V_o(\omega)}{A_{in}(\omega)} = \frac{-j \frac{2Y_c dt_c b^*}{a\varepsilon}}{2\zeta\omega^2 + j \left[\omega_n^2 k^2 + \frac{2\zeta\omega_n^2}{R_L C_P} \right]} \quad (2.32)$$

The electrical power delivered to the load is given by V_o^2/R_L . Substituting the expression for V_o from 2.32, yields the following result for the output power at the resonance frequency [32]

$$P = \frac{1}{\omega^2} \frac{R_L C_P^2 \left(\frac{2Y_c dt_c b^*}{a\varepsilon} \right)^2}{(4\zeta^2 + k^4)(R_L C_P \omega)^2 + 4\zeta k^2 (R_L C_P \omega) + 2\zeta^2} A_{in}^2 \quad (2.33)$$

The optimum load resistance that maximizes the output power is obtained by solving $\frac{\partial P}{\partial R_L} = 0$. This yields the following result [32]

$$R_{L_{opt}} = \frac{1}{\omega C_P} \frac{2\zeta}{\sqrt{4\zeta^2 + k^4}} \quad (2.34)$$

The electrical damping factor defined in section 2.1 can also be determined using for a piezoelectric device using the above model. The result is stated here [32]

$$\zeta_E = \frac{\omega k^2}{\sqrt{\omega^2 + \frac{1}{(R_L C_P)^2}}} \quad (2.35)$$

It is important to note that ζ_E becomes equal to ζ (Mechanical damping factor) when $R_L = R_{L_{opt}}$. This is in agreement with the maximum power condition for the generic vibration based harvester in section 2.1

2.2.3 Simplified Resonance Model

Under steady state vibrations close to or at the resonance frequency of the device, the reactive elements in the primary of the transformer model cancel each other out, and it suffices to model the piezoelectric element as an AC current source in parallel with a resistor and capacitor as shown in Figure 2.7a [35] [32] [36]. The current source can be transformed into an equivalent voltage source using source transformation equations as shown in Figure 2.7b [36], where $V_P = I_P|Z|$ and $Z = R_P // \frac{1}{j\omega C_P}$

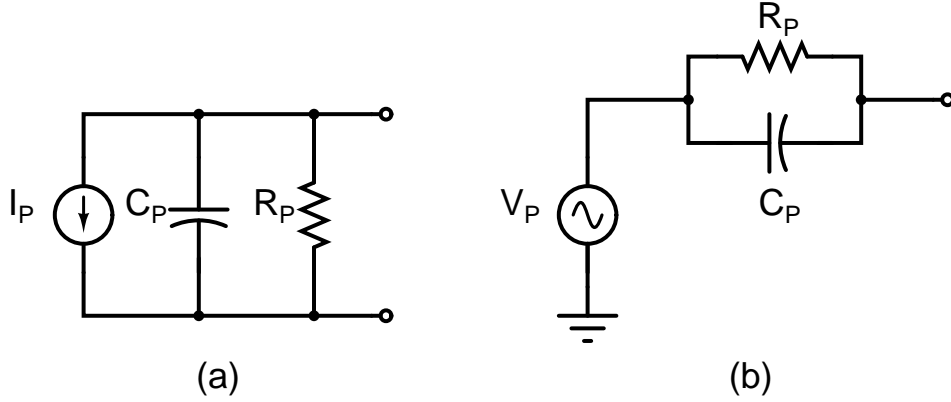


Figure 2.7: (a) Simplified model with current source model (b) Equivalent voltage source model

3. PIEZOELECTRIC HARVESTER INTERFACE CIRCUITS

In this section various piezoelectric harvester interface circuits in the literature are presented, highlighting their strengths and weaknesses. Most (if not all) piezoelectric harvester systems can be divided into three basic blocks: a rectifying element, a DC-DC converter and the load. The rectifier converts the AC output of the piezoelectric bender into DC, and the converter provides DC regulation as well as load impedance matching. A typical piezoelectric energy harvesting system is depicted in Figure 3.1. Maximizing output power requires a careful look at the following considerations:

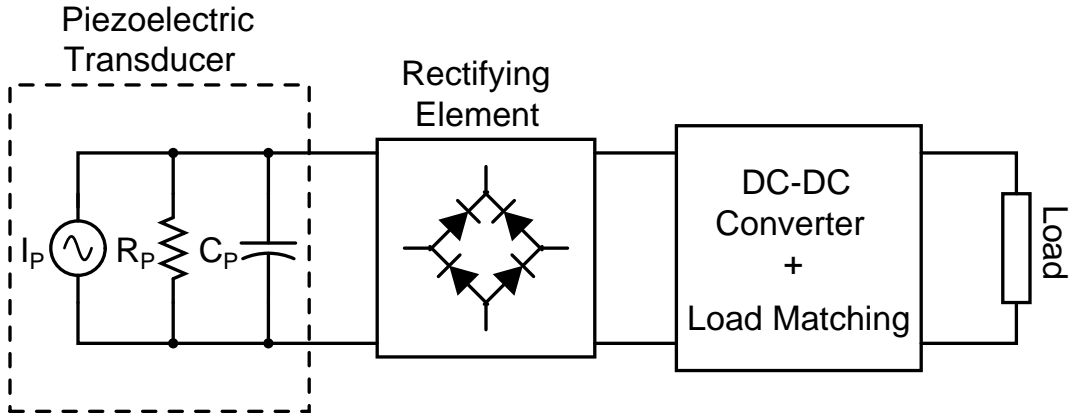


Figure 3.1: Typical piezoelectric energy harvesting system

- Minimizing losses in each of the stages
- Ensuring proper load impedance matching
- Reducing "dead time" in load current due to rectifier non-idealities

Many rectifier implementations exist each with its own strengths and weaknesses. The maximum power point varies across topologies. Topologies whose maximum power points exist at higher voltages are generally more preferable as they obviate the need for an additional boost stage. The basic building block for most rectifying stages is the diode bridge. The diodes could be replaced with MOSFET switches to reduce the losses in the rectifier due to diode forward drop, although this approach requires additional circuitry.

3.1 Full-Wave Bridge Rectifier

Perhaps the simplest method of extracting energy from a piezoelectric device is to connect it through a full wave rectifier to a storage/smoothing capacitor which may be used as an input to a DC-DC converter stage [35]. A typical implementation is shown in Figure 3.2. The smoothing/storage capacitor C_{RECT} is assumed to be

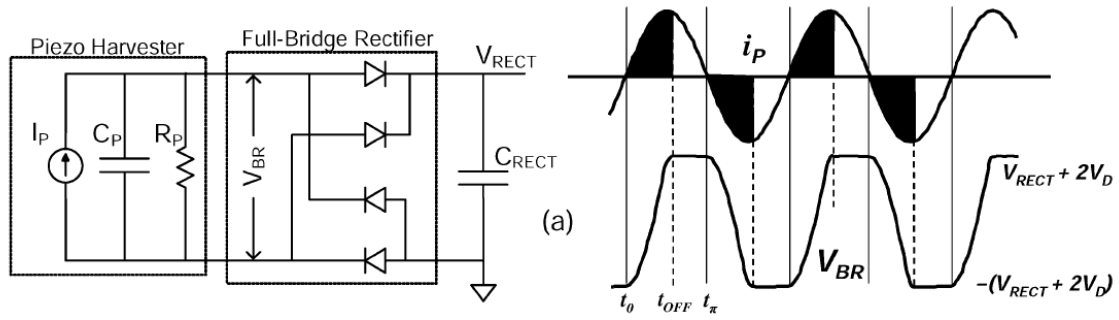


Figure 3.2: Full wave rectifier ©IEEE 2010 [8]

much larger than C_P so that the output voltage stays relatively constant at V_{RECT} . Under these conditions, the voltage and current waveforms for sinusoidal excitation ($i_P = I_P \sin \omega t$) is shown on the left of Figure 3.2. The current waveform is made up of two regions: the "dead time" from t_0 to t_{OFF} during which all of the current i_P goes

to charge or discharge the capacitor C_P to provide the appropriate bias to turn on the diodes. During this period all the diodes are reverse biased and there is no current to the load [8]. The second region is from t_{OFF} to t_π during which the capacitor C_P is either charged to $V_{RECT} + 2V_D$ or discharged to $-V_{RECT} - 2V_D$. Current flows from the piezoelectric device to the load during this period. The average load current is largely dependent on the length of the "dead time" which in turn depends on the voltage V_{RECT} . This means that the output power delivered will be dependent on the output voltage. The output power P is given by

$$P = \frac{I_P V_{RECT}}{\pi} \int_{\omega t_{OFF}}^{\pi} \sin(\omega t) d(\omega t) \quad (3.1)$$

$$= \frac{I_P V_{RECT}}{\pi} [\cos(\omega t_{OFF}) + 1] \quad (3.2)$$

t_{OFF} is simply the time it would take for C_P to charge from $-V_{RECT} - 2V_D$ to $V_{RECT} + 2V_D$. Assuming that all of the current i_P flows into the C_P during this interval (neglecting the current through R_P),

$$\Delta V_{BR} = \frac{I_P}{\omega C} \int_0^{\omega t_{OFF}} \sin(\omega t) d(\omega t) \quad (3.3)$$

The change in capacitor voltage over this interval is $\Delta V_{BR} = V_{RECT} + 2V_D - (-V_{RECT} - 2V_D) = 2(V_{RECT} + 2V_D)$. Substituting into 3.3, we have

$$2(V_{RECT} + 2V_D) = \frac{I_P}{\omega C_P} [1 - \cos(\omega t_{OFF})] \quad (3.4)$$

from which

$$\cos(\omega t_{OFF}) = 1 - \frac{2\omega C_P (V_{RECT} + 2V_D)}{I_P} \quad (3.5)$$

Substituting 3.5 into 3.2, rearranging and using $\omega = 2\pi f$, we have

$$P = 4V_{RECT}fC_P(V_P - V_{RECT} - 2V_D) \quad (3.6)$$

where $V_P = I_P/\omega C_P$. It can easily be shown by solving $\frac{\partial P}{\partial V_{RECT}} = 0$ that the power is maximum when $V_{RECT} = V_P/2 - V_D$. Substituting this value of V_{RECT} into 3.6 gives the following expression for the maximum power.

$$P_{MAX} = fC_P(V_P - 2V_D)^2 \quad (3.7)$$

A plot of output power versus rectifier output voltage is shown in Figure 3.3

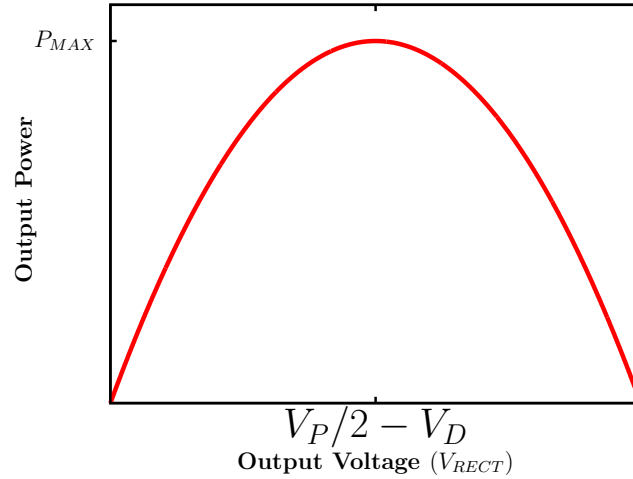


Figure 3.3: Output power vs output voltage for full wave rectifier

3.1.1 Switch-Only Rectifier

The main power bottleneck in the conventional bridge rectifier for piezoelectric energy harvesters is the dead-time in output current during which the terminal ca-

capacitance of the piezoelectric device C_P charges from $-V_{RECT} - 2V_D$ to $V_{RECT} + 2V_D$ or discharges from $V_{RECT} + 2V_D$ to $-V_{RECT} - 2V_D$. The switch-only rectifier [8] was proposed to minimize this dead-time. The rectifier and relevant voltage and current waveforms are shown in Figure 3.4. The dead time in load current for the

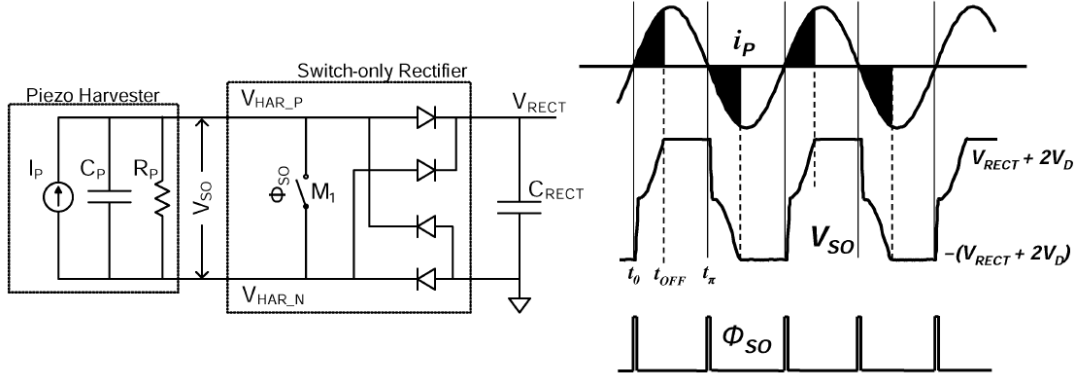


Figure 3.4: Switch-only rectifier ©IEEE 2010 [8]

full-bridge rectifier is simply the time required for the voltage across the piezoelectric device capacitance to change by $2(V_{RECT} + 2V_D)$ every time the current i_P changes direction. In the switch-only rectifier, the switch M_1 is closed every time the device current changes direction to quickly discharge(charge) the capacitor C_P from $V_{RECT} + 2V_D$ ($-V_{RECT} - 2V_D$) to ground. After the switch opens, the device current i_P only has to charge the capacitor by $\pm(V_{RECT} + 2V_D)$. If the switch ON resistance is negligible, the initial discharge(charge) by the switch occurs almost instantaneously, essentially halving the load current dead time as compared to the full bridge rectifier in which the voltage across C_P has to change by twice as much. Following a similar approach used in the full-bridge rectifier, it can be shown that the output power for

this topology is given by [8]

$$P = 2V_{RECT}fC_P(2V_P - V_{RECT} - 2V_D) \quad (3.8)$$

which reaches its maximum when $V_{RECT} = V_P - V_D$. The maximum power is given by

$$P = 2fC_P(V_P - V_D)^2 \quad (3.9)$$

It should be noted that the maximum power point for this rectifier is about twice that for the conventional full-bridge topology, making higher output voltages possible. Also the maximum power is twice the maximum power for the full-bridge rectifier. This topology will however require additional control circuitry to generate the control signals for the switch.

3.1.2 Full Wave Rectifiers with Switched Inductors

As explained in the above sub-section, the dead time in load current that occurs during commutation creates a considerable reduction in output power even at the maximum power point. It follows that the output power can be increased by reducing the commutation interval. The dependence of the commutation interval on the parasitic terminal capacitance of the piezoelectric device C_P suggests that it can be drastically reduced (theoretically eliminated) by resonating out C_P at the frequency of operation. This is however not a feasible approach as the inductor sizes required become impractical, especially for low frequency vibrations. For example for a device with $C_P = 50nF$ vibrating at 200Hz, the required inductance is about 12.67H. Switching the inductor into circuit only during the commutation interval allows smaller inductors to be used to the same effect [8]. The "switched inductor" essentially increases the commutation speed thereby reducing load current dead-time.

The approach is implemented in [33] [9] and in the so called bias-flip rectifier [8] in which the inductor is also shared with a buck converter following the rectification stage. The technique is shown in Figure 3.5 The output power of the above rectifier

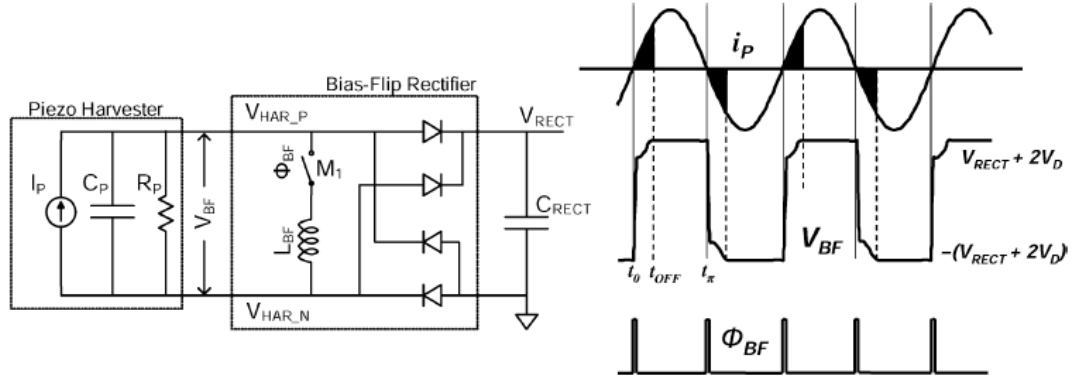


Figure 3.5: Bias-flip rectifier and relevant waveforms ©IEEE 2010 [8]

is given by [8]

$$P = 2C_P V_{RECT} f (2V_P - (V_{RECT} + 2V_D)(1 - e^{-\tau})) \quad (3.10)$$

where $\tau = \pi\beta/\omega$, $\omega = R_{BF}/2L_{BF}$, $\omega = \sqrt{\omega_o^2 - \beta^2}$ and $\omega_o = 1/L_{BF}C_P$. The technique provides considerable improvement in output power compared to the standard full wave rectifier, with a possible increase of up to 12.55X [8] using ideal diodes. The maximum power point is also higher than that of the full bridge rectifier, making it amenable to high voltage systems. A discrete implementation known as the Parallel SSHI(Synchronous Switched harvester on Inductor) was presented in [9, 33, 37]. A 2.6X improvement over the conventional full bridge rectifier was recorded. The Series SSHI technique is also presented in [37] [9] in which the switched inductor is

placed in series with the rectifier as shown in figure 3.6 (a). With this technique

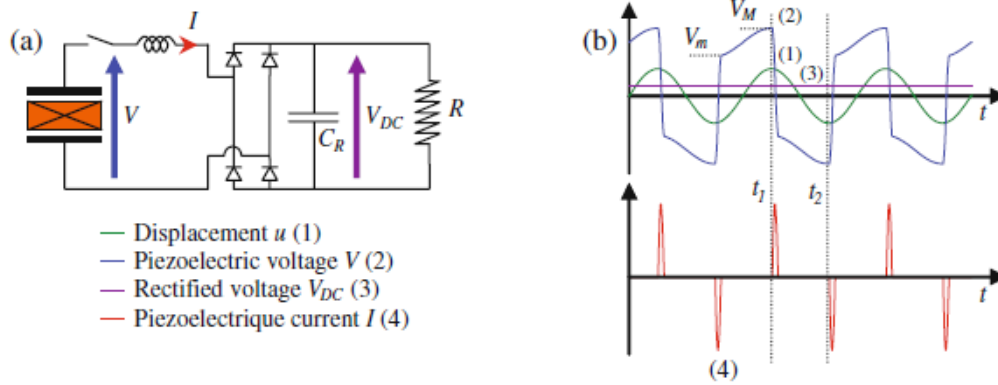


Figure 3.6: (a) Series SSHI technique (b) Relevant waveforms [9]

the piezoelectric current is always null except during voltage inversion during which the inductor is switched into circuit. The load current therefore consists of narrow pulses that occur every half cycle as shown in Figure 3.6 (b). The maximum output power obtainable using this method can be very close to the Parallel case for very short inversion(commutation) intervals. The maximum power point (output voltage for which power output is maximized) is however higher for the parallel case.

3.2 Voltage Doubler

The voltage doubler [36,38] is another commonly used rectifier topology. A typical implementation is shown in Figure 3.7. In this topology, the load current flows only during the positive cycle. During the negative half cycle, the diode connected across the piezoelectric devices turns on, and the voltage across C_P is essentially $-V_D$. When the current becomes positive, i_P charges C_P from $-V_D$ to $V_{RECT} + V_D$ at which point the diode connected to the storage capacitor turns on and current flows

to the load. The output power delivered for this topology can be shown to be [8]

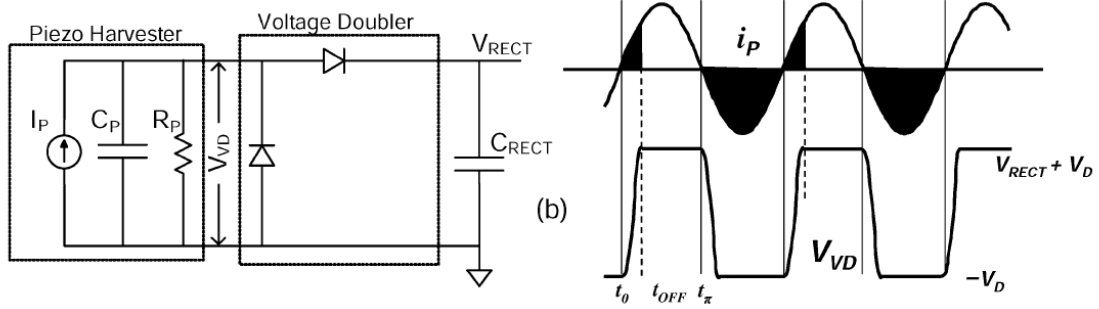


Figure 3.7: Voltage doubler ©IEEE 2010 [8]

$$P = V_{RECT} f C_P (2V_P - V_{RECT} - 2V_D) \quad (3.11)$$

which is exactly half of the output power of the switch-only rectifier. As with the switch-only rectifier, the output power is maximized when $V_{RECT} = V_P - V_D$, at which point the output power is

$$P = f C_P (V_P - V_D)^2 \quad (3.12)$$

It should be noted that the effect of R_P was neglected in all power derivations. Detailed derivations which take into account the effect of R_P can be found in Appendix B of [39]. In the presence of ideal diodes, the output power of the voltage doubler is the same as that for the full-bridge rectifier but the voltage doubler pushes the output voltage required for maximum output power to 2X that for the full-bridge rectifier [8].

It was shown in the previous chapter that the output power is maximized when

electrical damping matches mechanical damping, from which the optimum load resistance that achieves this was derived. This suggests a need to present the appropriate load impedance at the output of a rectifier (which translates to keeping the output at the correct voltage). The problem is addressed in [35, 40, 41] where switching stages with feedback loops are included after the rectifier to hold its output at the optimum voltage while providing a regulated output voltage.

3.3 Synchronized Energy Charge Extraction

All the rectifier based extraction techniques discussed in this section (with the exception of the series SSHI technique) are most effective for narrow band excitation. They however become ineffective for broad band excitations. Another drawback of these techniques is the dependence of output power on output voltage, a dependence that necessitates some kind of output voltage feedback to ensure maximum power point tracking [35]. The Synchronous Energy Charge Extraction (SECE) [9] tech-

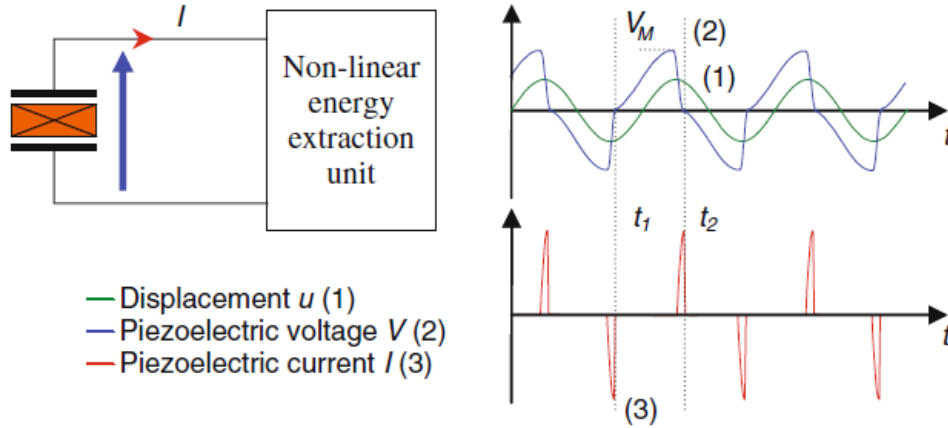


Figure 3.8: Synchronous energy charge extraction technique and relevant waveforms [9]

nique which is more suitable for broadband excitations, and whose output power is less dependent on output voltage is presented in this sub-section. A functional view of the technique is shown in Figure 3.8. It is a non-linear technique, which involves extracting energy from the piezoelectric device at the peak of its displacement, which corresponds to the peak of the device terminal voltage, or peak of the voltage across the piezoelectric device capacitance C_P . The energy stored in C_P , which is maximum at this point, is quickly transferred to the load causing C_P to quickly discharge to zero. The process is then repeated for the negative half cycle. Since the capacitor voltage alternates between positive and negative values from one half cycle to another, some kind of rectification is needed to ensure DC output current. A "rectifier-free" technique was implemented in [42] [10] which achieves unidirectional current without the use of a conventional bridge rectifier at the input. The schematic of the implementation is shown in Figure 3.9. The control circuit (not shown here)

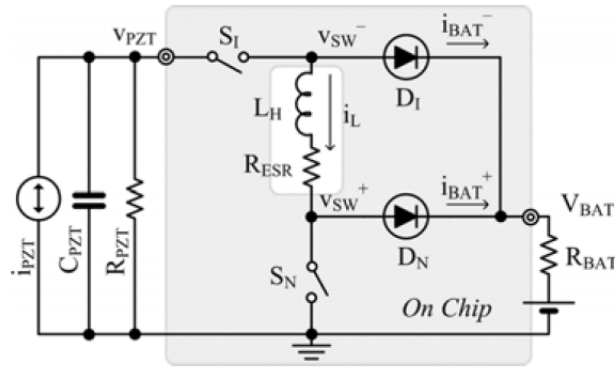


Figure 3.9: Rectifier-free piezoelectric energy harvester using SECE ©IEEE 2010 [10]

detects the peak of v_{PZT} which corresponds to the peak of the device displacement and closes S_1 and S_N . The energy stored in C_{PZT} quickly transferred to the inductor

L_H causing v_{PZT} to fall to 0. S_N is then opened (S_1 is opened for the negative half cycle) and the voltage v_{SW}^+ quickly rises to forward bias the diode D_N causing the inductor to discharge into the battery. The battery is charged through D_1 for the negative half cycle. Neglecting the losses through the diodes and switches (i.e. assuming all the power accumulated by C_{PZT} is transferred to the load), it can easily be shown [10] [9] that the output power is given by

$$P = \frac{I_P^2}{\pi^2 f C_P} \quad (3.13)$$

Using the substitution $V_P = I_P / 2\pi f C_P$ and accounting for the diode drop V_D , 3.13 becomes

$$P = 4f C_P (V_P - V_D)^2 \quad (3.14)$$

This is four times the maximum output power obtainable from a conventional full bridge rectifier based harvester (a full bridge rectifier operating at its maximum power point). Unlike the rectifier based harvesters, the power output with the SECE technique is independent of the output voltage. No correcting loop is required to keep the output voltage at the maximum power point. The SECE implementation in [10] has the additional advantage of not having a minimum input amplitude requirement. The inductor automatically raises v_{SW}^+ and v_{SW}^- to whatever value is required to turn on the diodes D_1 and D_N , making it possible to harvest energy from very low amplitude vibrations. The results forgoing results for selected interface circuits are summarized in Table 3.1.

3.4 Initial Energy Injection

The interface circuits that have been treated so far in this chapter have unidirectional energy flow i.e. energy flows from the piezoelectric generator (PEG)

Table 3.1: Comparison of selected piezoelectric interface circuits

| | P_{MAX} | MPP | Input Threshold |
|-----------------------|----------------------|---------------|------------------|
| Full Bridge Rectifier | $fC_P(V_P - 2V_D)^2$ | $V_P/2 - V_D$ | $V_{OUT} + 2V_D$ |
| Voltage Doubler | $fC_P(V_P - V_D)^2$ | $V_P - V_D$ | $V_{OUT} + V_D$ |
| Switch-only Rectifier | $2fC_P(V_P - V_D)^2$ | $V_P - V_D$ | $V_{OUT} + 2V_D$ |
| SECE [10] | $4fC_P(V_P - V_D)^2$ | N/A | N/A |

to the load and never in the reverse direction. It can be shown [9, 11, 43], that a significant output power enhancement can be obtained by pulsed energy flow in the reverse direction. The enhancement is based on the fact that the energy stored in a capacitor is proportional to the square of the voltage across it. Suppose the PEG charges its parasitic capacitance C_P from 0 to V_C after the positive half cycle. The energy accumulated in the capacitor after charging is $\frac{1}{2}C_P V_C^2$. If, however, the capacitor is initially charged to V_B before being further charged by the PEG to $V_B + V_C$, the energy stored in the capacitor after being charged by the PEG becomes

$$E = \frac{1}{2}C_P(V_C^2 + V_B^2 + 2V_C V_B) \quad (3.15)$$

This energy is made up of three components: the initial energy stored in the capacitor due to initial bias $\frac{1}{2}C_P V_B^2$, the energy generated by the PEG with no initial bias $\frac{1}{2}C_P V_C^2$, and the energy enhancement due to the initial bias $C_P V_C V_B$ which is proportional to the initial bias provided. Of course for the technique to be beneficial, the initial energy injection process should be highly efficient, specifically, the energy

lost in creating the initial bias should be less than the output power enhancement due to the technique. Under such conditions, and general minimum loss conditions in the main power path, the power gain compared to standard bridge rectifier harvesters can theoretically reach 4000% [11]. The increase in transducer's electrostatic energy creates an increase in its terminal voltage which in turn leads to more harvested power. The output voltage therefore increases allowing for more energy to be injected, and hence more harvested energy in the next cycle. The pulsed energy

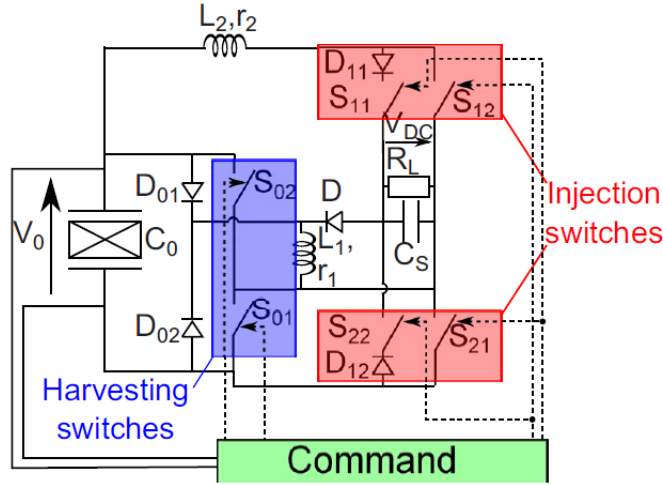


Figure 3.10: Initial energy injection (discrete implementation) [11]

feedback therefore creates some kind of "energy resonance" effect [11] allowing for more harvested energy in each cycle. The effect is however limited by the losses in both the injection circuit and the main power transfer path. A discrete implementation of the principle is shown in Figure 3.10. The electrostatic energy stored on the device reaches its maximum at the extrema of its terminal voltages. At this point energy is harvested from the device to the storage capacitor C_S through the inductor

L_1 which acts as an intermediate storage device. Immediately after the harvesting process, a fraction of the harvested energy is injected back into the device through the inductor L_2 . The inductor is used to minimize losses in the injection path as its efficiency is critical to the overall functioning of the system. The above system was reported [11] to have harvested up to 20X more energy than the conventional bridge rectifier using off-the-shelf components.

A fully integrated implementation of the initial energy injection principle was reported in [12]. An overview of the system is depicted in Figure 3.11. The harvester

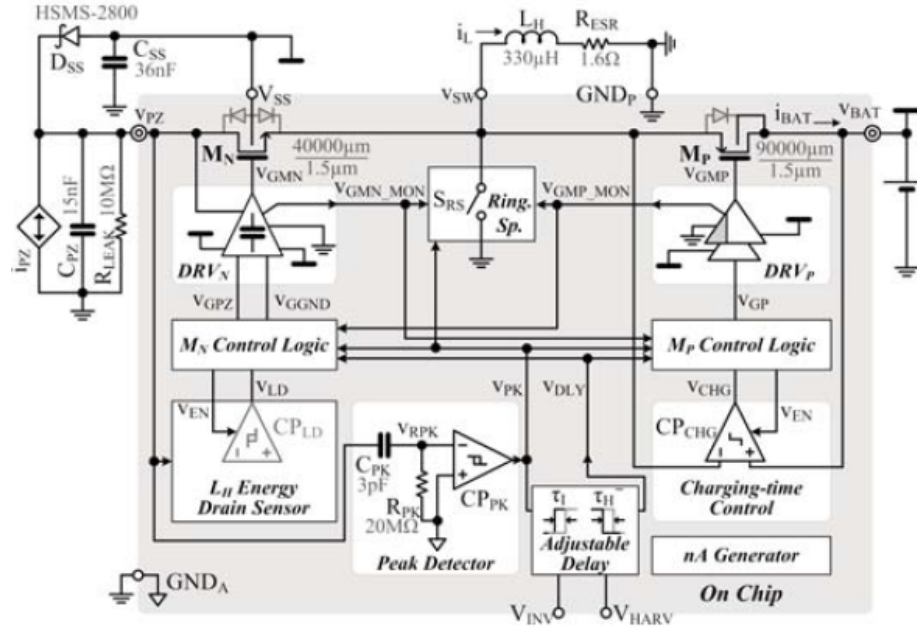


Figure 3.11: Energy-investing piezoelectric energy harvesting system ©IEEE 2013 [12]

‘invests’ some energy from the battery to pre-charge the PEG at the beginning of every half cycle (end of every positive half cycle). The invested energy along with the energy gains due to the initial charge are extracted at the end of the negative

half cycle.

The "energy resonance" effect described earlier in the section was used to interesting effect in [13]. The energy from the transducer was repeatedly transferred to an intermediate inductor and back, increasing the initial voltage bias of the transducer after each cycle. The process is repeated until the transducer voltage reaches the process breakdown voltage, at which point harvesting begins. The voltage across the terminals of the piezoelectric device is maintained close to the breakdown voltage of the process, maximizing the energy harvested from the device. The system and the "pile-up" resonance effect are depicted in Figures 3.12 and 3.13. Theoretically

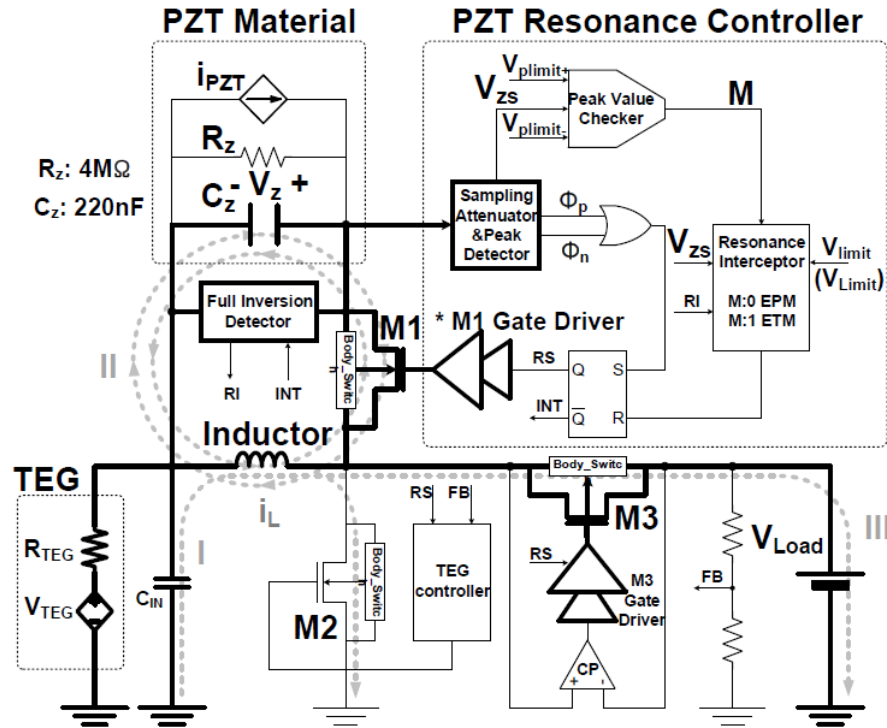


Figure 3.12: Energy pile-up resonance piezoelectric energy harvesting system ©IEEE 2014 [13]

the amount of energy that can be harvested using this approach is limited by the breakdown voltage of the process. A 422% improvement in output power over the conventional full-bridge rectifier was reported in [12].

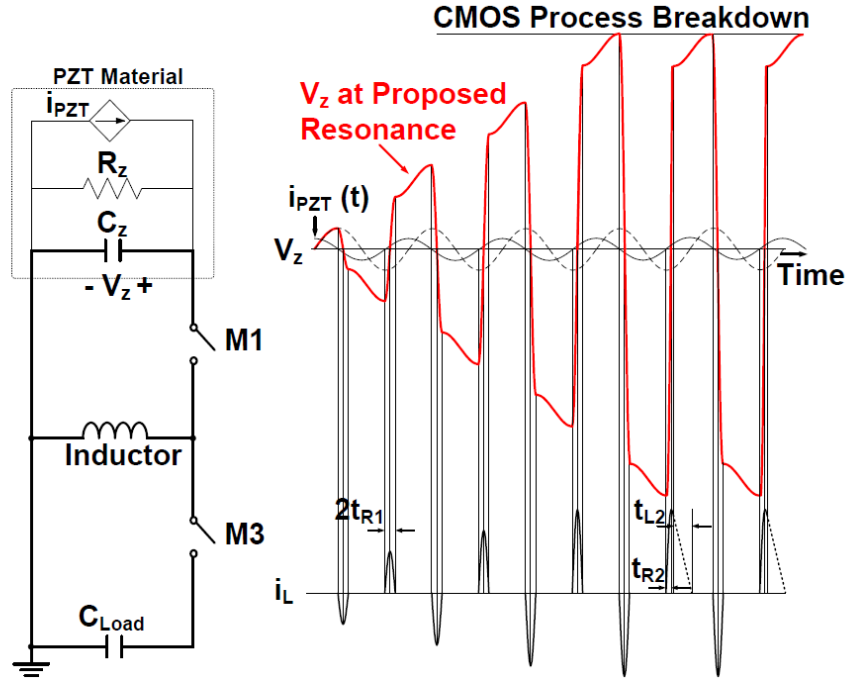


Figure 3.13: Energy pile-up resonance effect ©IEEE 2014 [13]

4. PIEZOELECTRIC HARVESTER DESIGN

4.1 Motivation and System Overview

The alternating nature of piezoelectric device current makes the connection of multiple strips in series or parallel, while still maximizing power output non-trivial. This is especially so when the devices vibrate asynchronously. To illustrate, let us consider three different piezoelectric devices vibrating at their resonant frequencies and connected in parallel as shown on the left in Figure 4.1.

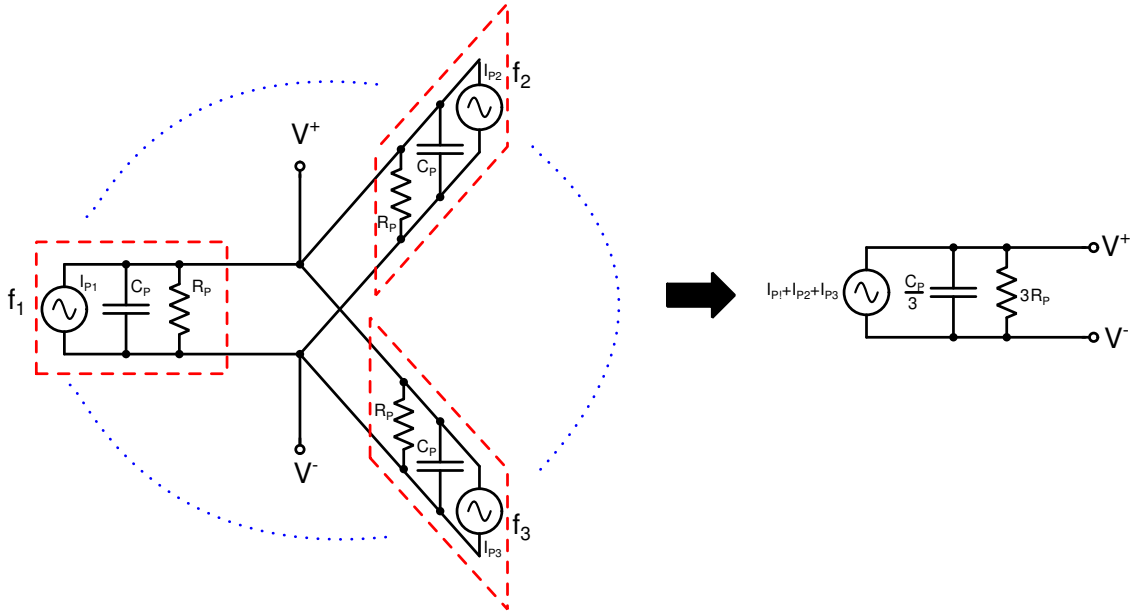


Figure 4.1: Connection of multiple piezoelectric devices in parallel

Assuming, for simplicity, that the device terminal impedances are equal, the parallel connection of three devices could theoretically be modeled as a single device with current $I_T = I_1 + I_2 + I_3$, resistance $R_P/3$ and capacitance $3C_P$ vibrating at

its resonant frequency as shown on the right in figure 4.1. Let $I_1 = I_{P1} \sin \omega_1 t$, $I_2 = I_{P2} \sin \omega_2 t$, and $I_3 = I_{P3} \sin \omega_3 t$. An important observation can be made from the various interface circuits analyzed in the previous chapter: the power output in each topology is proportional to the rms current of the input piezoelectric device. This presents an interesting challenge for multiple input systems. If all the devices are vibrating at the same frequency, that is if $\omega_1 = \omega_2 = \omega_3 = \omega$, then the equivalent current I_T is simply $(I_{P1} + I_{P2} + I_{P3}) \sin \omega t$ whose the rms value is given by

$$I_{TRMS} = \frac{I_{P1}}{\sqrt{2}} + \frac{I_{P2}}{\sqrt{2}} + \frac{I_{P3}}{\sqrt{2}} = I_{RMS1} + I_{RMS2} + I_{RMS3} \quad (4.1)$$

Thus the rms values of the currents add up linearly when the devices vibrate synchronously. For the case where $\omega_1 \neq \omega_2 \neq \omega_3$ however, the rms current is given by

$$I_{TRMS} = \sqrt{\frac{I_{P1}^2}{2} + \frac{I_{P2}^2}{2} + \frac{I_{P3}^2}{2}} = \sqrt{I_{RMS1}^2 + I_{RMS2}^2 + I_{RMS3}^2} \quad (4.2)$$

which is always less than rms current obtained when the devices vibrate synchronously. The above relations hold for vibrations occurring in phase. For asynchronous vibrations however, the combination of currents can be destructive leading to a reduction in output power. In particular, two sources vibrating 180° out of phase produces zero output power. This is illustrated in Figure 4.3. This could be avoided by using multiple harvesting paths as shown in Figure 4.2. While this mitigates the reduction in power output, the use of multiple harvesters, each with its own set of components would prove costly in terms of quiescent power and PCB real estate. The approach becomes impractical when a large number of input devices (and frequencies) are involved. This work presents a harvester that effectively combines the power from multiple piezoelectric devices vibrating at multiple asynchronously using a single

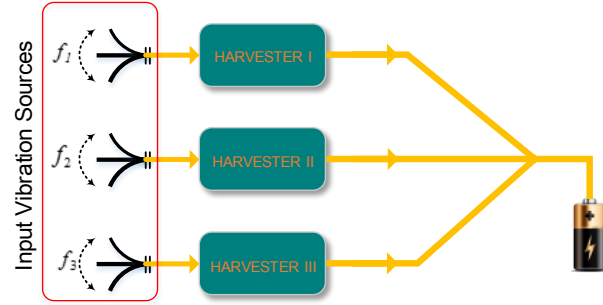


Figure 4.2: Parallel harvesting paths

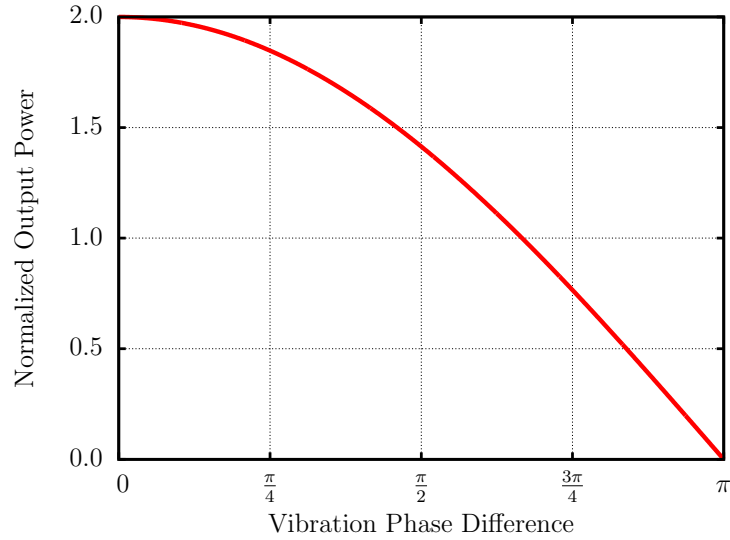


Figure 4.3: Normalized power vs vibration phase difference for two inputs

inductor. A conceptual view of the proposed system is shown in Figure 4.4. The approach is based on the utilization of the relatively long "fallow" periods in inductor current in the SECE technique. The sparsity of inductor current spikes creates long periods of zero inductor current which could potentially be used to extract energy

from other devices.

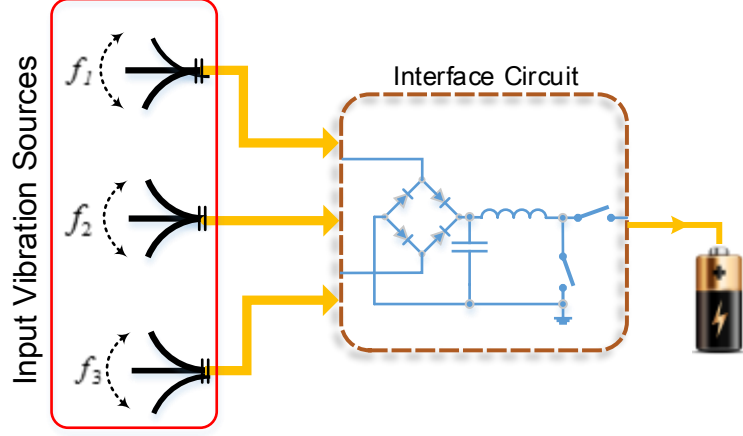


Figure 4.4: Conceptual view of the system

4.2 System Architecture and Design

As stated in the previous section the proposed multiple input topology is based on the SECE technique. The rectifier free topology presented in [12] was used as the basic building block due to the absence of a minimum input voltage threshold requirement. The schematic of the topology is shown in Figure 4.5. The circuit extracts energy from the device at the peak of the device displacement which corresponds to the peak of the voltage V_{PZT} . The control circuit(not shown here) detects this voltage peak and closes the switches S_1 and S_{GND} to transfer the energy accumulated in the capacitor C_P over the positive half cycle to the inductor L . All of the capacitor's energy is transferred to the inductor after approximately one-fourth of the resonance period ($0.5\pi\sqrt{LC_P}$), at which point V_{PZT} falls to zero (C_P is fully discharged) and the inductor current I_L reaches its peak. The capacitor is allowed

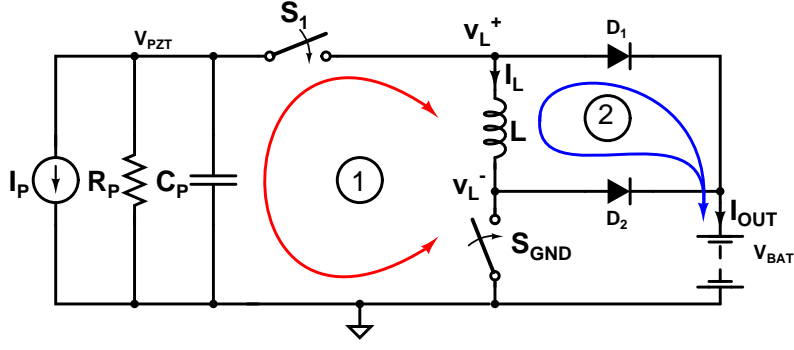


Figure 4.5: Rectifier-free SECE topology

to further discharge below ground to create an initial bias for C_P , thereby increasing the energy extracted in the next half cycle as was shown in the previous chapter. The amount of initial bias that can be applied is however limited by the breakdown voltage for the technology. After the creating the initial bias, S_{GND} opens, while the inductor current is non-zero. This attempt to interrupt the inductor current causes the inductor to raise the voltage at v_L^- thereby forward biasing D_1 and discharging the inductor into the battery. S_1 opens after the inductor has been fully discharged. The process repeats for the negative half cycle with the inductor discharging through D_2 after S_1 opens. The voltage and current waveforms along with the control signals for S_1 and S_{GND} are shown in Figure 4.6. The harvesting interval τ_L is usually in the order of a few micro-seconds which is very negligible compared to vibration periods τ_{VIB} typically in the order of milliseconds. The inductor therefore lies idle for most of the vibration period and can be used to harvest energy from other piezoelectric devices independently from each other. This is implemented in a three input piezoelectric energy harvesting system shown in Figure 4.7 Since the harvesting paths operate orthogonally (independently from each other) the total power supplied to the load is simply the linear sum of the power extracted from each

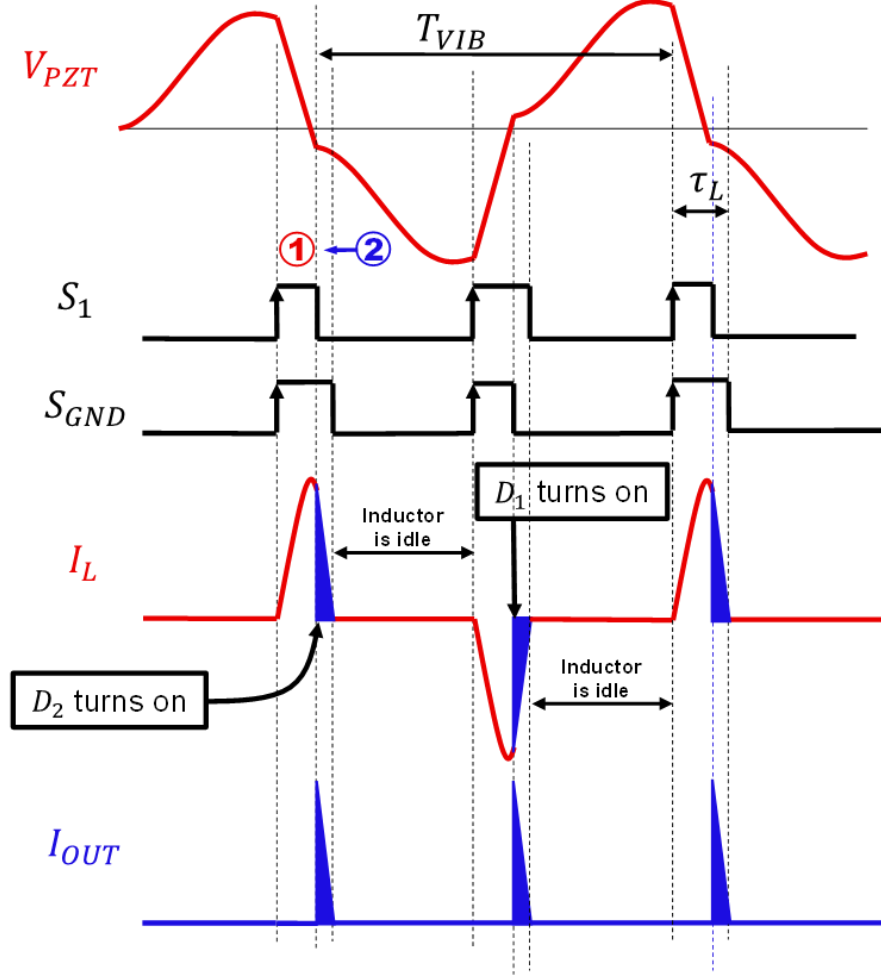


Figure 4.6: Waveforms for V_{PZT} , I_L and I_{OUT} and switch control signals

path. The power output for the SECE topology was derived in the previous chapter as

$$P = \frac{I_P^2}{\pi^2 f C_P} = 4C_P V_P^2 \quad (4.3)$$

For N devices vibrating independently, the total power will be

$$P = \frac{1}{\pi^2} \sum_{i=1}^n \frac{I_{Pi}^2}{f_i C_{Pi}} \quad (4.4)$$

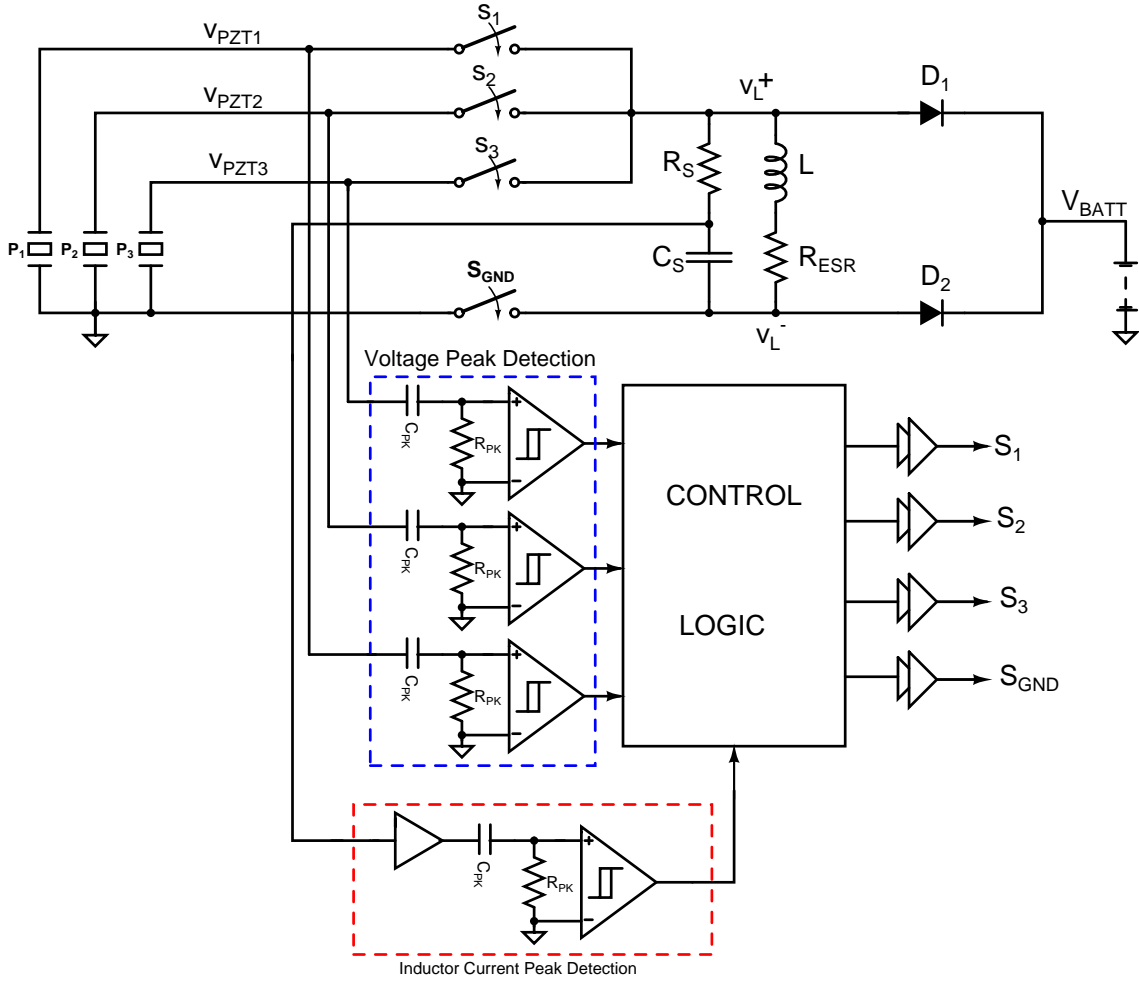


Figure 4.7: Proposed system architecture

The switches are independently synchronized to the peaks of the voltages V_{PZT1} , V_{PZT2} and V_{PZT3} allowing for power extraction from each of the devices using the same inductor.

4.2.1 Voltage Peak Detection

The SECE technique harvests energy from the device at the peak of the device displacement which corresponds to the peak of the device terminal voltages. A robust peak detection circuit is therefore required to ensure proper operation. The

peak detection scheme is depicted in Figure 4.8. The differentiator extracts the slope

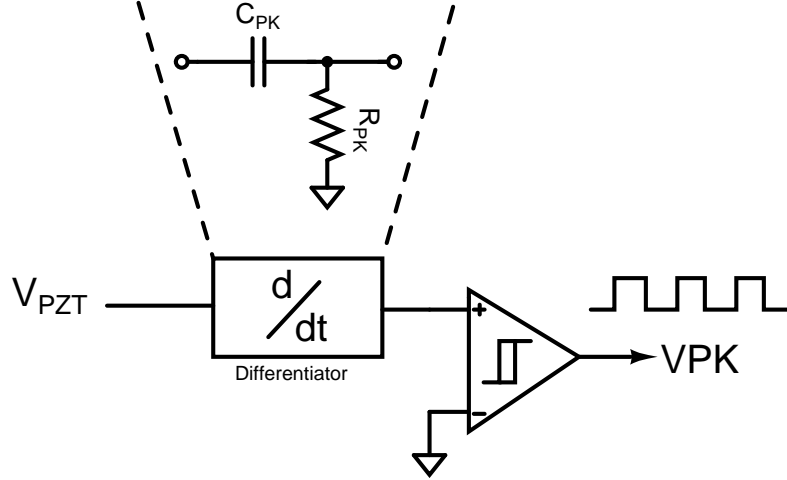


Figure 4.8: Voltage peak detection

of V_{PZT} and the comparator detects the sign changes in the slope which represent the peaks of V_{PZT} . A change from positive to negative slope corresponds to a positive peak, and a change from negative to positive slope corresponds to a negative peak. The output of the comparator is therefore a square wave whose rising edge corresponds to a negative peak and whose falling edge corresponds to a positive peak. The differentiator is implemented with a passive high pass filter to minimize power consumption. The transfer function is given by

$$H(s) = \frac{sC_{PK}R_{PK}}{1 + sC_{PK}R_{PK}} \approx sC_{PK}R_{PK}, \quad \omega \ll \frac{1}{C_{PK}R_{PK}} \quad (4.5)$$

Thus for frequencies much lower than the pole frequencies, the filter essentially acts as a differentiator. The harvester was designed to for vibration frequencies up to 300Hz. Thus the pole frequency was chosen to be 30MHz, to ensure that the high

the peak detector over a wide range of input voltages. Sub-threshold design was employed to minimize quiescent current in the analog building blocks. The transistor sizes are summarized in Table 4.1. Figure 4.10 is the simulated transfer curve of

Table 4.1: Comparator transistor sizes

| Transistor | Dimension(μm) |
|------------|----------------------|
| M_1 | 8/0.9 |
| M_2 | 8/1 |
| M_3 | 4/1 |
| M_4 | 2/1 |
| M_5 | 4/2 |
| M_6 | 20/2 |
| M_{H1} | 12/1 |

the comparator showing a hysteresis window of about 40mV. The output of the peak detector showing a transition at every peak(or minimum) is shown in Figure 4.11.

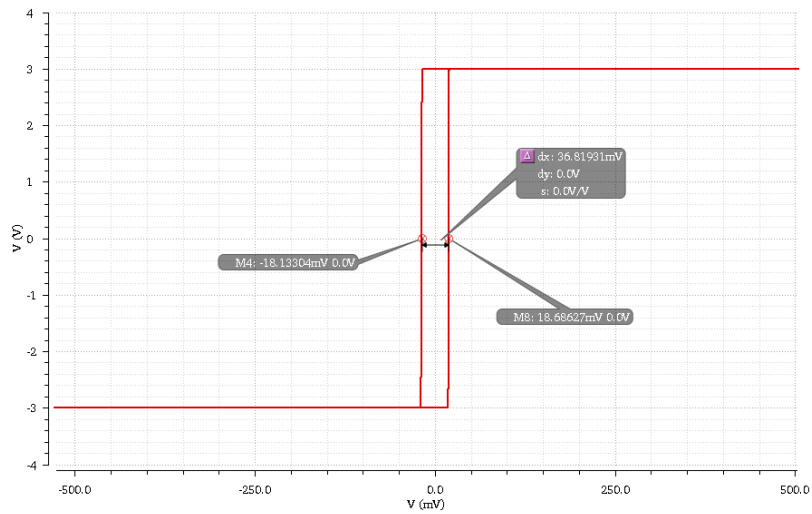


Figure 4.10: Comparator transfer characteristic

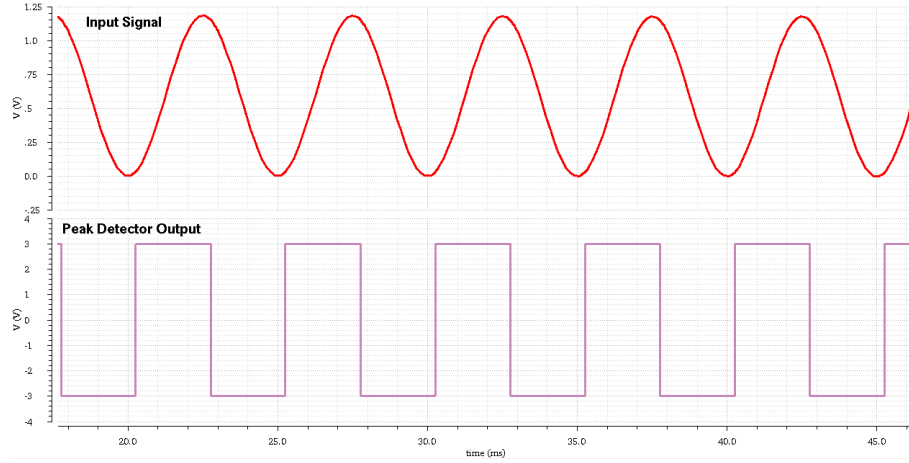


Figure 4.11: Peak detector output

4.2.2 Comparator Bias Current Generator

The bias current was generated using the supply independent PTAT(Positive To Absolute Temperature) current generator shown in Figure 4.12. The circuit has two stable operating points, one at $I_{IN} = I_{OUT} = 0$, and the desired non-zero operating point. The first operating point exists at startup and the circuit would remain there without a startup circuit. Transistors $M_{S1} - M_{S5}$ serve as a startup circuit, introducing some current at startup to move the circuit to the desired operating point. The startup circuit becomes inactive after the desired operating point is reach. It can be shown [44] that the current I_{OUT} under steady state conditions is given by

$$I_{OUT} = \frac{V_T \ln 2}{R_{BIAS}} = \frac{0.693 \times V_T}{R_{BIAS}} \quad (4.7)$$

Setting $I_{BIAS} = 15nA$ in 4.7 gives $R_{BIAS} = 0.6M\Omega$

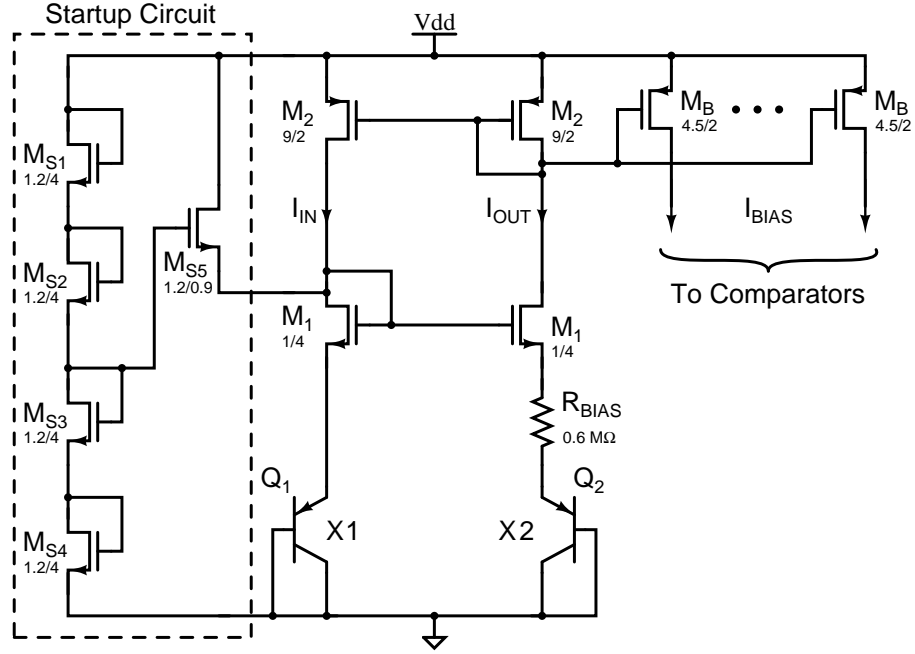


Figure 4.12: Bias current generator

4.2.3 Inductor Current Sensing

The inductor current was sensed using the lossless current sensing scheme presented in [45]. This employs a passive lowpass filter to filter the inductor voltage as shown in Figure 4.13. The output of the filter can be made to be proportional to the inductor by selecting an appropriate time constant for the filter. This is illustrated in the following analysis. The output of the lowpass filter V_S is related to the input voltage V_L by the filter transfer function. Thus

$$V_S = \frac{V_L}{1 + sR_S C_S} \quad (4.8)$$

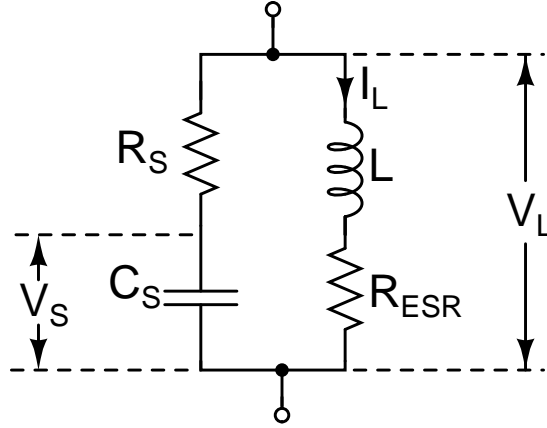


Figure 4.13: Inductor current sense network

Using $V_L = I_L(R_{ESR} + sL)$, we have

$$V_S = I_L R_{ESR} \frac{1 + s \frac{L}{R_{ESR}}}{1 + s R_S C_S} = I_L R_{ESR} \frac{1 + s \tau_1}{1 + s \tau_2} \quad (4.9)$$

where $\tau_1 = \frac{L}{R_{ESR}}$ and $\tau_2 = R_S C_S$. Equation 4.9 becomes $V_S = I_L R_{ESR}$ when $\tau_1 = \tau_2$. Thus the voltage V_S becomes proportional to the inductor current when the time constants are closely matched. For a $200\mu H$ inductor with ESR of 3Ω the required time constant is $66.67\mu s$. This was matched using a $1k\Omega$ resistor in series with a $66.67nF$ capacitor. The inductor and the output voltage of the sense network are shown in Figure 4.14. The output of the current sensor is fed into a peak detector. The peak detector outputs a square waveform whose edges correspond to the peaks of the inductor current.

4.2.4 Control Block

A top level view of the control block is shown in Figure 4.15. The switch control signals are generated using state machines(SCB_1-3) that are synchronized to the edges of the voltage peak detection output. A pair of signals are generated from

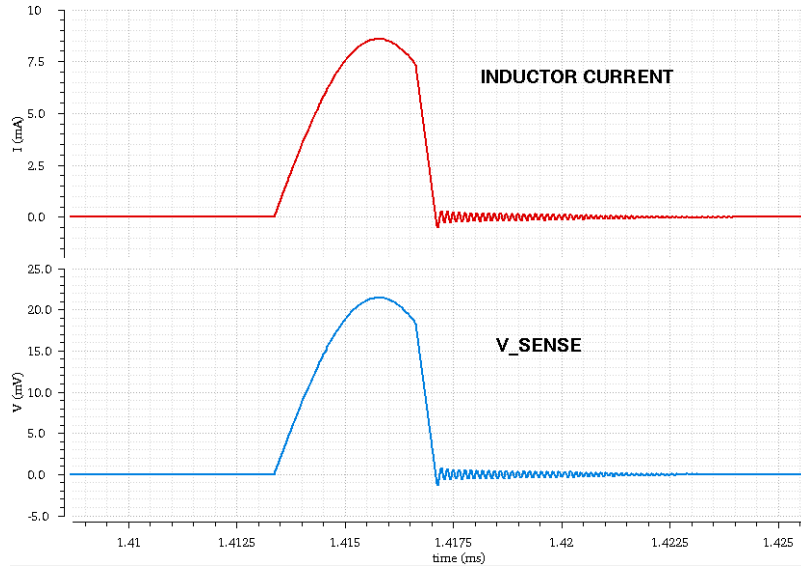


Figure 4.14: Inductor current and sense voltage

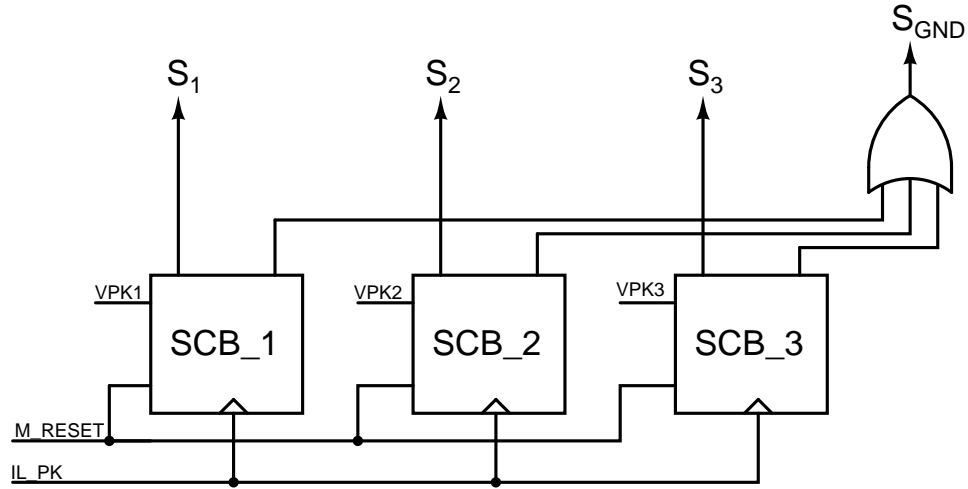


Figure 4.15: Control block

each state machine for each transducer. Since all the transducers share a common negative terminal which is connected to ground, a single switch S_{GND} is used between v_L^- and ground as shown in Figure 4.7. The control signal for this switch is obtained

by combining the ground switch signals for each of the inputs through an OR gate. The Gate level implementation of the state machine is shown in Figure 4.16. It consists of two D flip-flops with the D inputs connected to '1'. The flip-flops are synchronized to the output of a pulse generator which generates short pulses at both edges of the signal $VPKN$ as shown in Figure 4.17. The width of the pulses is $2\tau_D$. The flip-flops are reset at the peak of the inductor current. The combination of the

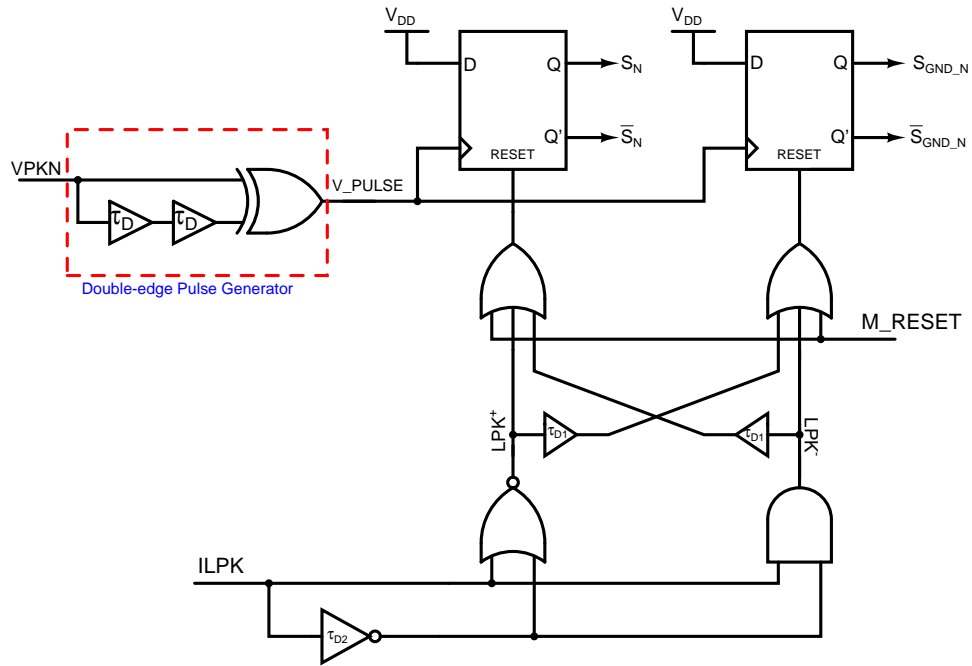


Figure 4.16: State machine

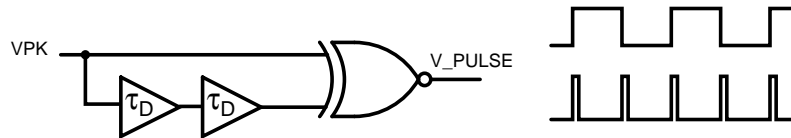


Figure 4.17: Double edge pulse generator

NOT gate and the NOR gate generates short pulses of width τ_{D2} at the rising edge of ILPK, and that of the NOT gate and the AND gate generates identical pulses at the falling edge of ILPK. A master reset signal M_RESET is used to reset the flip-flops at startup. A pulse is generated at the peak of the input signal and applied to the clock input of the flip-flop causing the signals S_N and S_{GND_N} to go high. At the positive peak of the inductor current, a pulse is generated at the output of the NOR gate (the output of the AND gate remains unchanged) to reset the first flip-flop causing S_N to go to low while S_{GND_N} remains high. A delayed version of the same pulse is used to reset the second flip-flop causing S_{GND_N} to go low τ_{D2} seconds after S_N . The reset order is reversed for the negative half cycle. The delay τ_{D2} is made to be larger than the inductor discharge time to ensure that all the energy from the inductor flows to the load before the switch is opened.

4.2.5 Switches and Active Diode

The switches play a very important role in improving the overall efficiency of the system and must therefore be carefully designed. The main design consideration is the minimization of the switch ON resistance, to minimize conduction (I^2R) losses while the switches are closed. The ON resistance of a MOSFET switch is typically given by

$$R_{ON} = \frac{1}{\frac{1}{2}\beta(V_{GS} - V_T)} \quad (4.10)$$

The ON resistance is therefore inversely proportional to the device aspect ratio and the overdrive voltage ($V_{GS} - V_T$). The resistance can therefore be minimized in two ways

- Increasing the sizes of the switch transistors
- Increasing the overdrive voltage of the switches during the ON state

Both approaches have limits beyond which they become impractical. Increasing device size increases the gate capacitance of the switches which in turn increases the amount of current required to turn them on, essentially increases switching losses. Since these losses are only incurred during switching, they are proportional to frequency. The energy required to charge the switch gate capacitance C_{GS} from $V_{GS(ON)}$ to $V_{GS(OFF)}$ is given by

$$E_{SW} = \frac{1}{2}C_{GS}(V_{GS(ON)}^2 - V_{GS(OFF)}^2) \quad (4.11)$$

Since switching occurs twice every cycle, the total losses due to switching over one cycle is just twice the result in 4.11. Multiplying the resulting switching loss per cycle by the frequency gives the switching losses as

$$P_{SW} = fC_{GS}(V_{GS(ON)}^2 - V_{GS(OFF)}^2) \quad (4.12)$$

As can be seen from the above result, the switching losses are proportional to the gate capacitance, which in turn depends on the transistor size, and frequency. The losses are also proportional to the square of the overdrive voltage. A direct trade-off therefore exists between switching losses and conducting losses. Minimizing conducting losses tends to increase switching losses and vice-versa. The type of loss that eventually dominates depends on the application. The general observation is that conduction losses dominate for high current low frequency applications, while switching losses dominate for low current high frequency applications. A sweet spot that minimizes the total losses (conduction + switching) usually exists and can be determined from simulation. A number of techniques (bootstrapping, parallel switching etc) are presented in the literature to minimize both types of losses. The optimum

transistor size for the switches were determined from simulation.

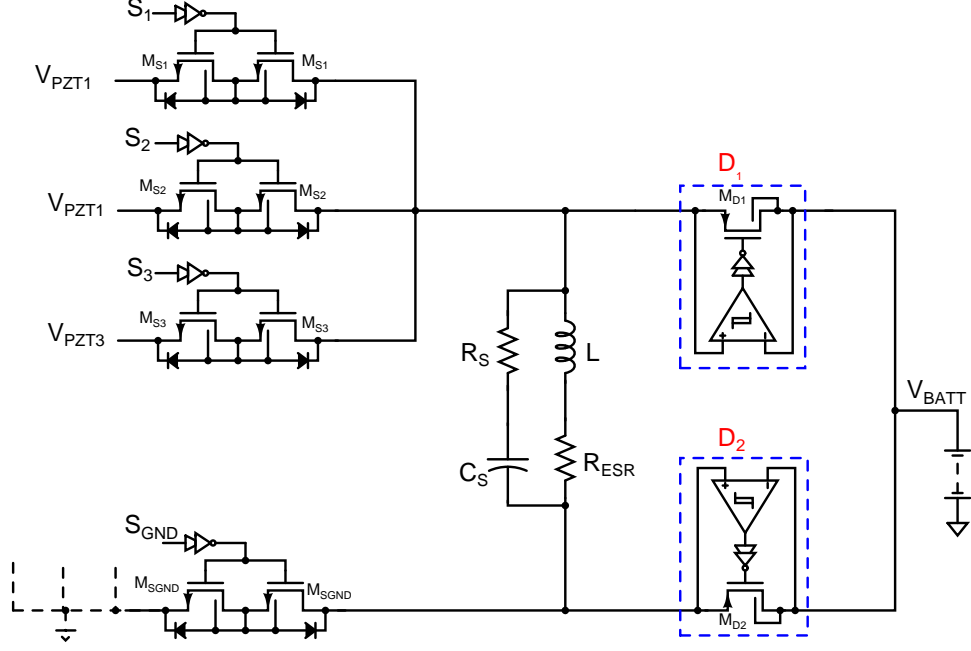


Figure 4.18: Switch implementation (transistor level)

The switch implementation is shown in Figure 4.18. Since the input voltages swing below ground, the body diodes of the NMOS switches could potentially turn on and conduct even when the switch is off. This problem is mitigated by using two switches connected in series so that their body diodes are connected back to back preventing body diode conduction even in the OFF state. The use of two switches in series increases conduction losses, although the increase is much less than the losses that would have been incurred through the body diode [12].

Synchronous rectifiers were used to avoid the losses that occur due to the forward drop of the diode. Many different topologies have been presented in the literature [46,46,47]. Most of these are however suited for high power applications and therefore

not suitable for this application. The approach used in [12] was used in this design. The conceptual view of a synchronous rectifier is shown in the highlighted portion of figure 4.18. The source and drain terminals of the pass transistor are connected to the input of a comparator whose output is connected to the gate of the same transistor. The output of the comparator goes low when $v_l > V_{BATT}$, turning on the transistor in the process. When $v_l < V_{BATT}$ the output of the comparator is high, turning off the transistor. The combination therefore acts as a diode without the forward drop. The schematic of the synchronous rectifier is shown in Figure 4.19.

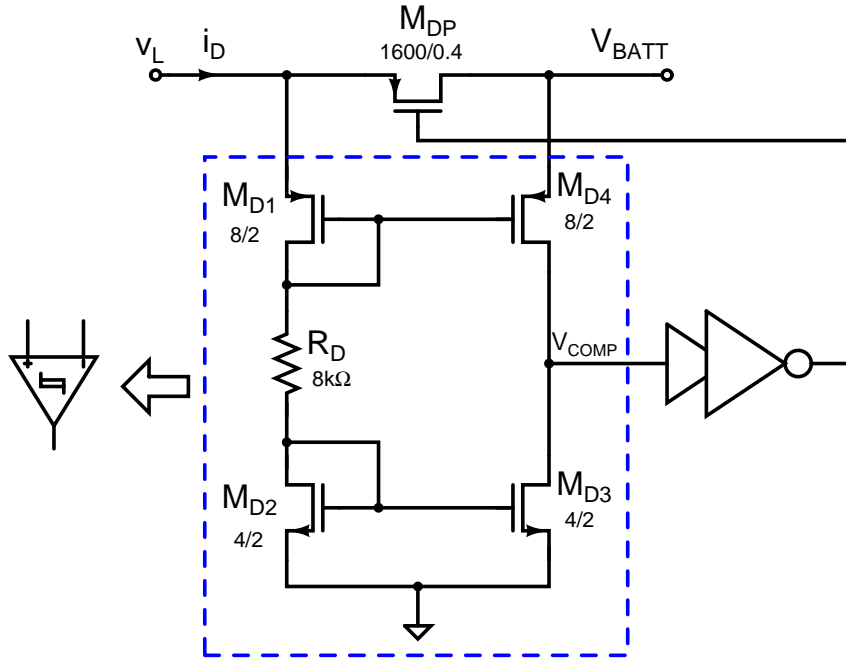


Figure 4.19: Synchronous rectifier

The highlighted portion of the circuit acts as a low power dynamic comparator, only consuming power when M_{DP} is on. In the OFF state, $i_D = 0$ so that the current through R_D , as well as the voltage drop across it are both zero. Also, the gate

source voltages of M_{D1} and M_{D2} are both zero pulling v_L to ground. The gate source voltage of M_{D4} is however equal to V_{BATT} . Since its drain current is zero, M_{D4} pulls V_{COMP} up to V_{BATT} , turning off M_{DP} . When i_D increases above zero, the parasitic capacitance at v_L charges above ground. Current starts to flow through M_{D1} and M_{D2} when v_L exceeds $V_{tn} + V_{tp}$. The current creates a voltage drop across R_D which pushes the voltage at the gates of M_{D1} and M_{D4} close to V_{BATT} essentially turning off M_{D4} , causing M_{D3} to pull V_{COMP} to ground. This turns on M_{DP} allowing current to flow to the battery. The simulation results for the active diode are shown in Figure 4.20. The inductor raises v_L^+ above V_{BATT} , causing V_{COMP} to fall to ground and

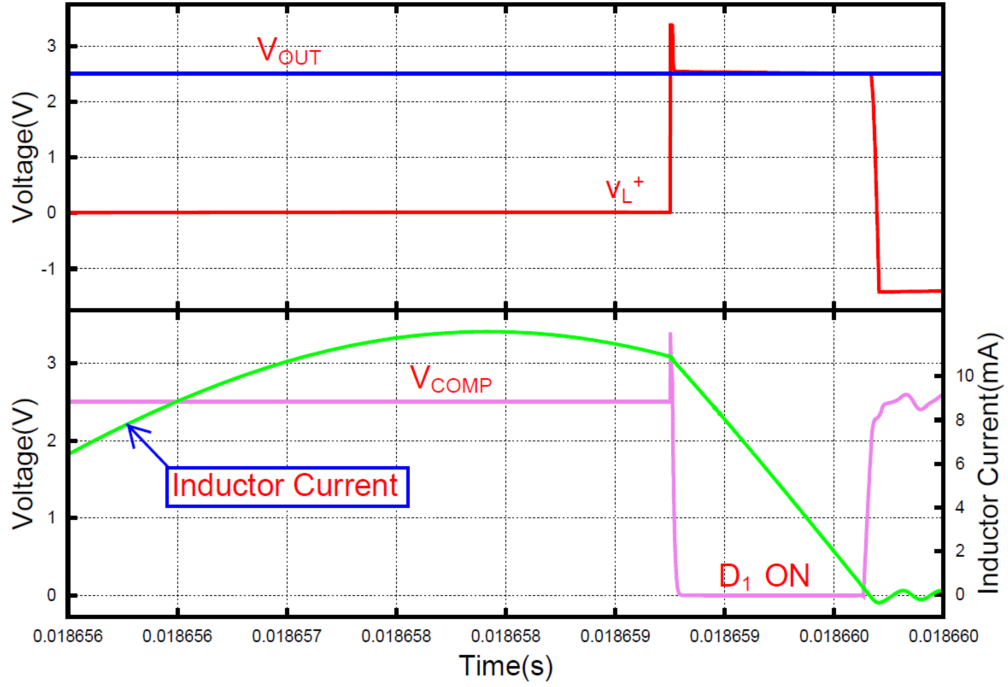


Figure 4.20: Active diode waveforms

thus turn on the diode. v_L^+ steadily falls while the inductor discharges into the load

capacitor/battery, reaching V_{BATT} when the inductor is almost fully discharged. At this point V_{COMP} goes to V_{BATT} turning off the diode.

4.2.6 Drivers, Delay Elements, and Level Converters

The typical voltage swings for $VPZT$ are around $\pm 1.5V - \pm 2V$. The gates of the switches will therefore have to be driven beyond these voltages to turn them on with minimum ON resistances. The switching signals from the state machines are however at CMOS levels and therefore unable to turn on the switches. The level converter circuit in Figure 4.21 is used to step up the output of the state machine from CMOS level to $V_{DD_HIGH} = 3.3V$ which is sufficient to turn on the switches for $VPZT$ amplitudes up to about $\pm 2.5V$. The series combination of switches

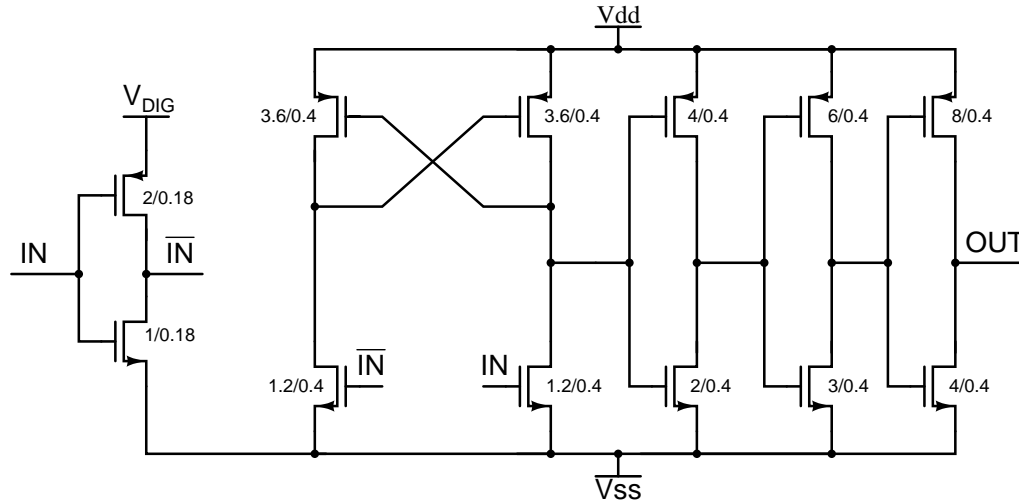


Figure 4.21: Level converter and gate driver

used to prevent body diode conduction creates large gate capacitances that cannot be driven by standard digital CMOS gates as they would be unable to source and sink the required current. The chain of inverters that follow the level converter are

appropriately sized to be able to source and sink the required current to drive the switches. The simulated input and output waveforms of the level converter are shown in Figure 4.22

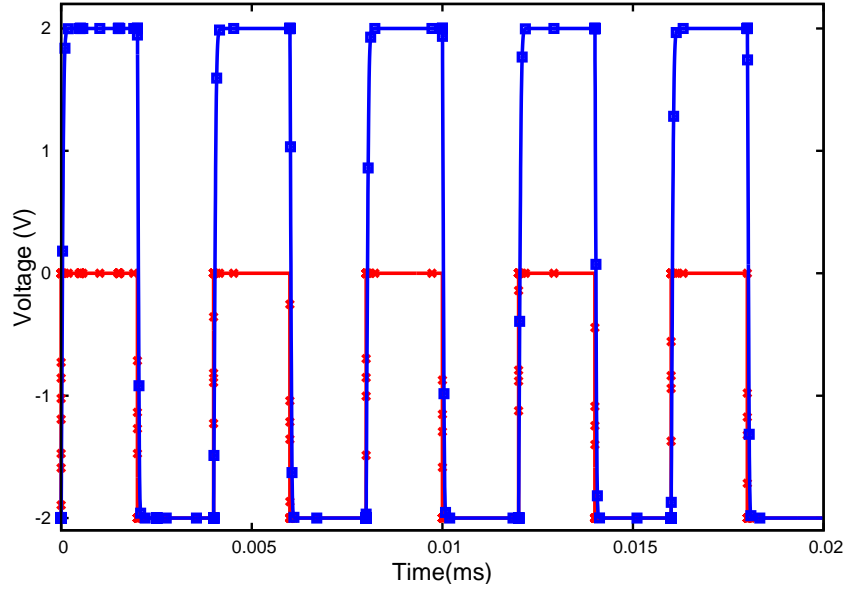


Figure 4.22: Level converter simulation results

4.3 Layout Considerations

Layout plays a very critical role in the performance of the fabricated circuit. Many deviations of measured results from simulation results can be attributed to bad layout techniques. A combination of careful planning and proper layout techniques were used to obtain the best layout possible. The layout techniques used were

- Extensive guard rings around sensitive analog blocks to minimize substrate coupling especially from high power gate drivers

- Interdigitization and common centroid to provide proper matching in all differential pairs and current mirrors
- Diffusion sharing for parallel transistors to minimize switch terminal capacitances (C_{GS}, C_{GD}, C_{DB})
- Wide metal paths on higher(thicker) metal layers were used for high current paths to minimize conduction losses due to path resistance.
- Separate power supply for digital circuits to prevent performance deterioration in supply sensitive analog blocks

The layouts of the various blocks as well as the entire chip are shown in Figures 4.23-4.28

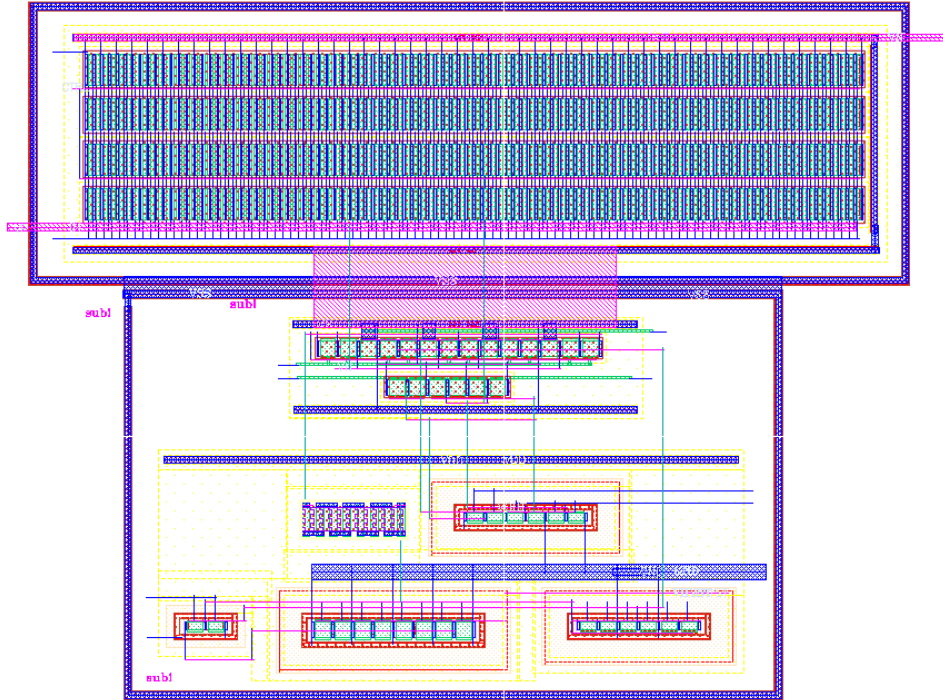


Figure 4.23: Layout of synchronous diode

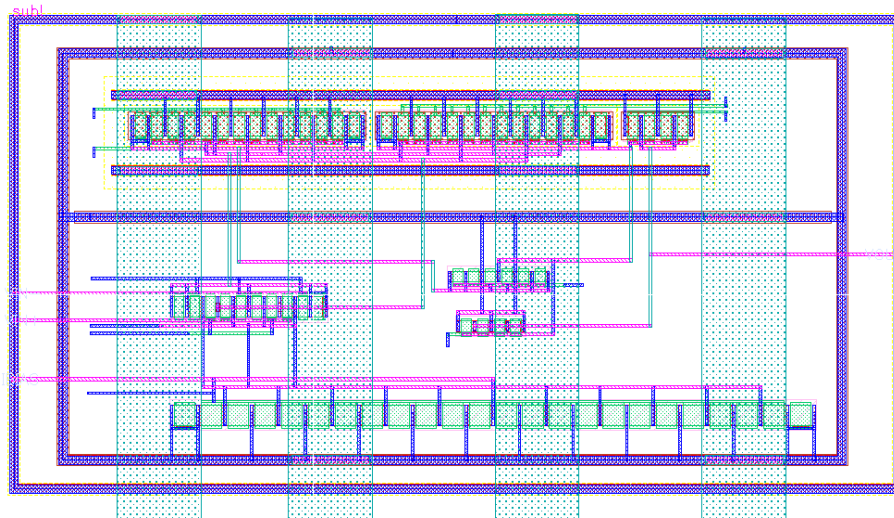


Figure 4.24: Layout of comparator

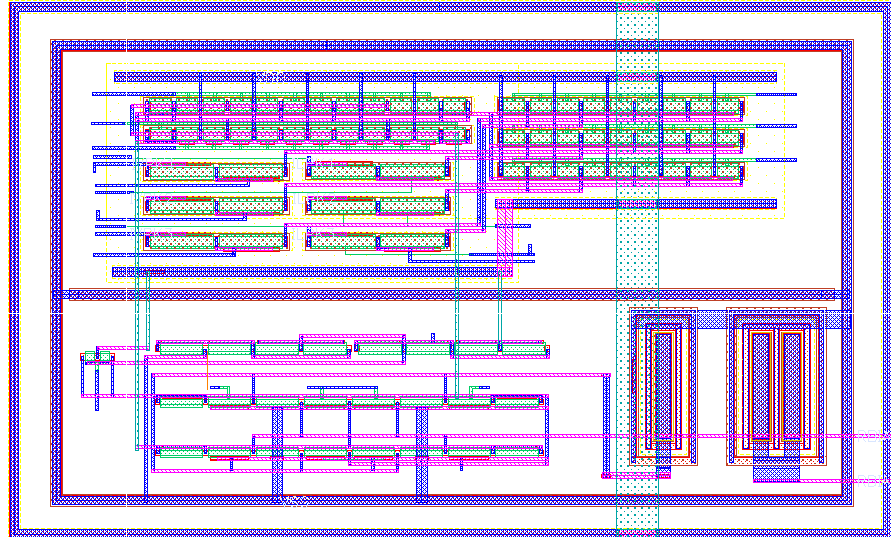


Figure 4.25: Layout of bias circuit



Figure 4.26: Layout of state machine

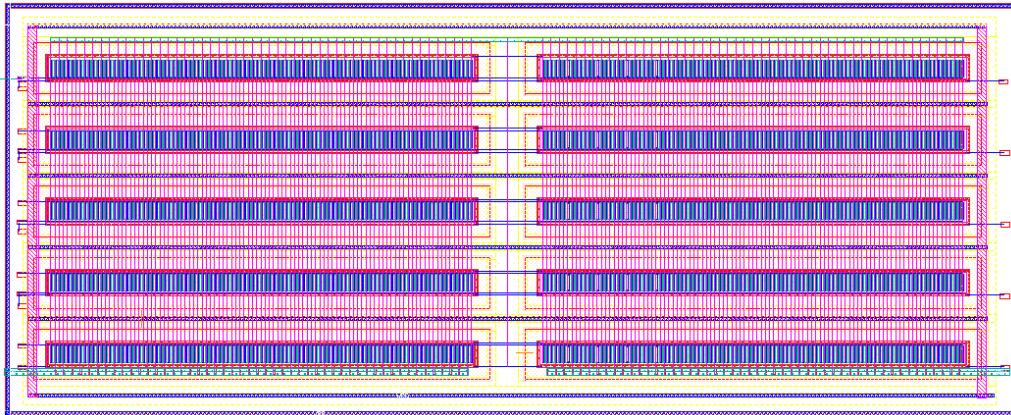


Figure 4.27: Layout of switch

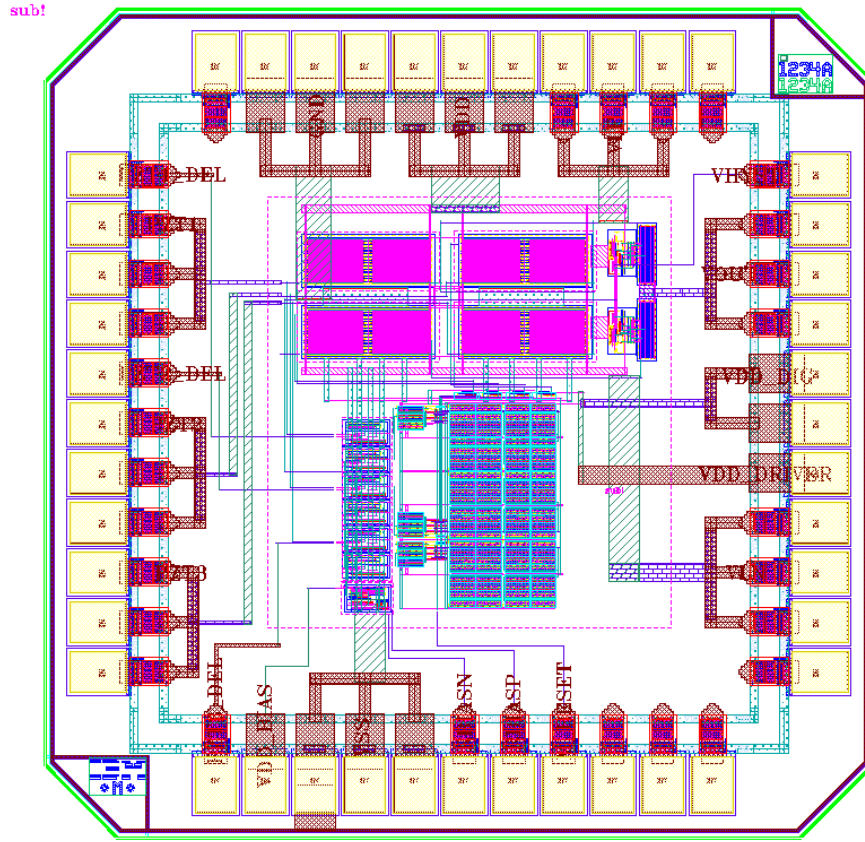


Figure 4.28: Layout of entire chip

4.4 Simulation Results

The system was simulated with three asynchronously vibrating input sources and a $400\mu F$ storage capacitor. The post-layout simulation results are shown in Figure 4.29. With the three asynchronously vibrating inputs the harvester was able to charge a $400\mu F$ capacitor by 1.8mV (from 2.5V to 2.5018V) in 30 milliseconds while consuming an average current of $2.2\mu A$ from $\pm 2.5V$. The parameters of the three input sources as well as the total available power output are outlined in Table 4.2. The energy transferred to the storage capacitor during the 30ms simulation interval

is

$$E_{OUT} = \frac{1}{2} \times 400 \times 10^{-6} \times (2.5018^2 - 2.5^2) = 1.8\mu J \quad (4.13)$$

which corresponds to an average power of $60\mu W$. The harvester consumes an average

Table 4.2: Summary of input sources in test bench

| f | $I_P(\mu A)$ | $C_P(\text{nF})$ | $R_P(k\Omega)$ | $P_{max}(\mu W)$ |
|--------------------------|--------------|------------------|----------------|------------------|
| 200 | 100 | 120 | 500 | 40.78 |
| 100 | 50 | 120 | 500 | 21.11 |
| 150 | 70 | 120 | 500 | 34.16 |
| Total Input Power | | | | 96.05 |

power of $5.5\mu W$. This gives a total efficiency of.

$$\eta = \frac{60}{96.05 + 5.5} \times 100 = 59.08\% \quad (4.14)$$

Figure 4.29 shows the simulated voltages at the terminals of the input devices as well as the inductor current and output voltage waveforms. A close up view of the waveforms during the harvesting interval is shown in Figure 4.30

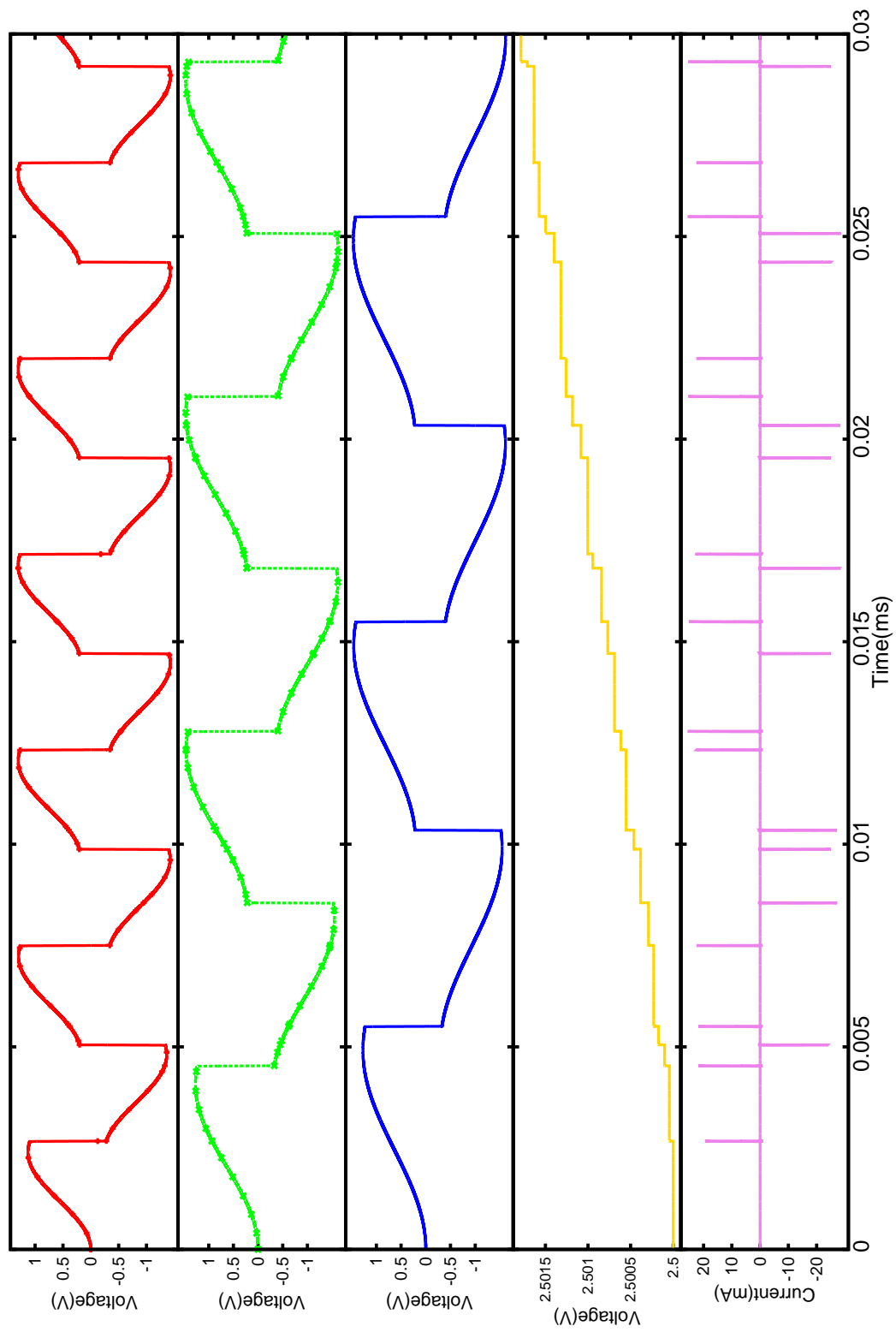


Figure 4.29: Post-layout simulation results

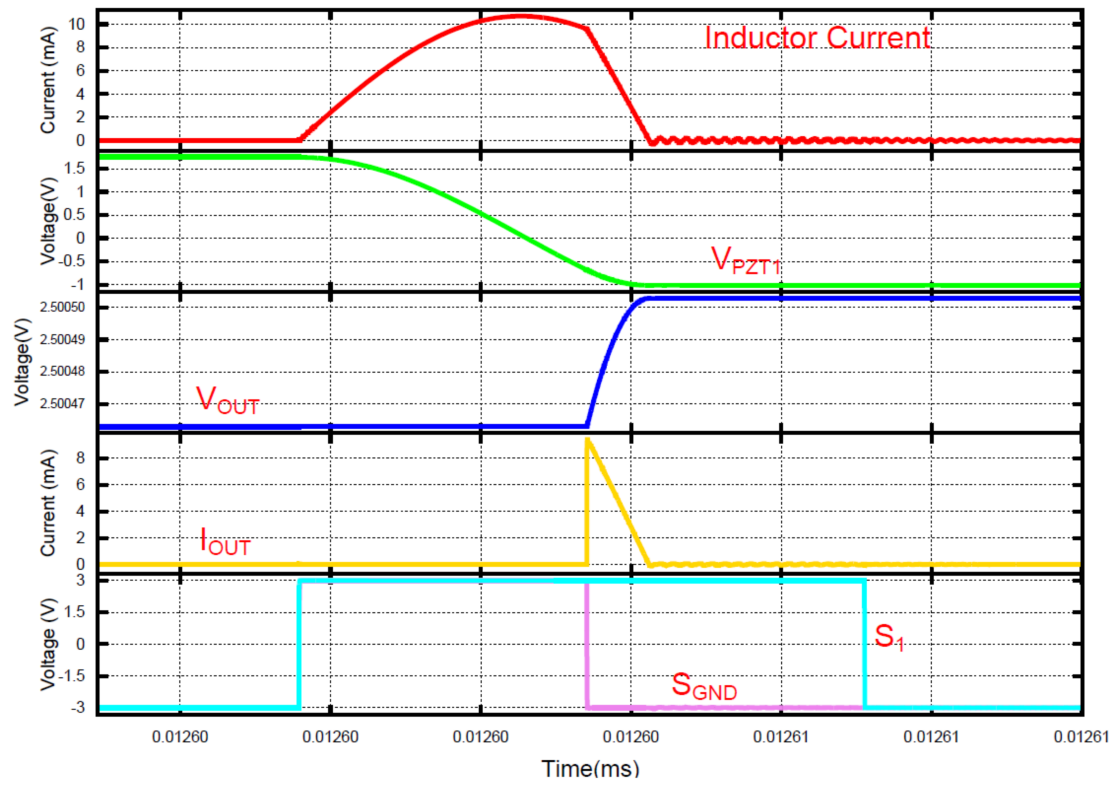


Figure 4.30: Close-up view of harvesting operation

5. EXPERIMENTAL RESULTS

The chip was successfully fabricated by MOSIS in the IBM $0.18\mu m$ technology, measuring $1500\mu m \times 1500\mu m$. The chip micrograph is shown in Figure 5.1. Testing was done with electrically modeled vibration elements to verify basic functionality, and to measure conversion efficiency. The basic resonance model presented in chapter 2 was used in testing. The experimental test setup is shown in Figure 5.2. The

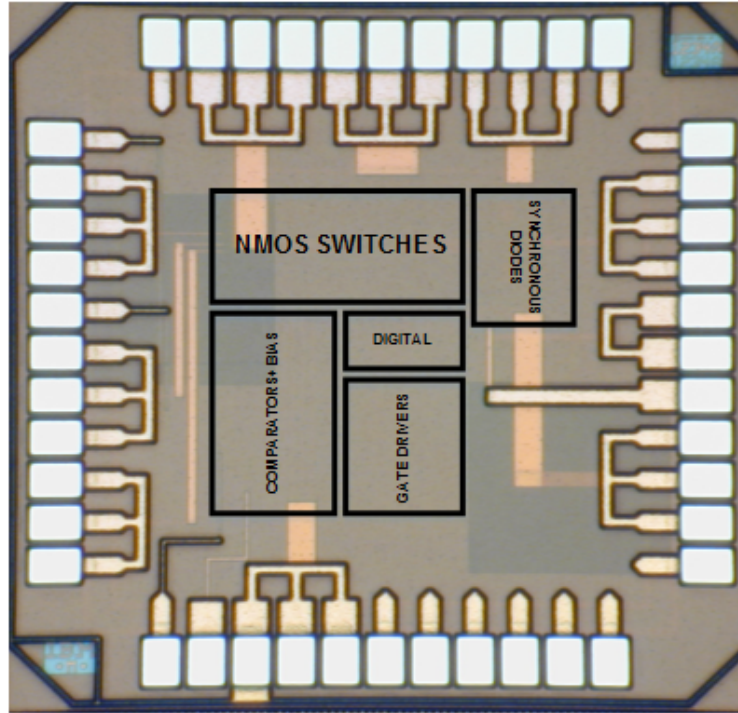


Figure 5.1: Die micrograph of interface chip

V22BL [48] piezoelectric harvester was used for preliminary mechanical testing. The results with modeled input vibrations are shown in Figure 5.3. The input vibration amplitude was limited to 5V to avoid high electrical stresses on the 3.3V devices for

sustained periods. The chip performs as expected, capturing energy from the input

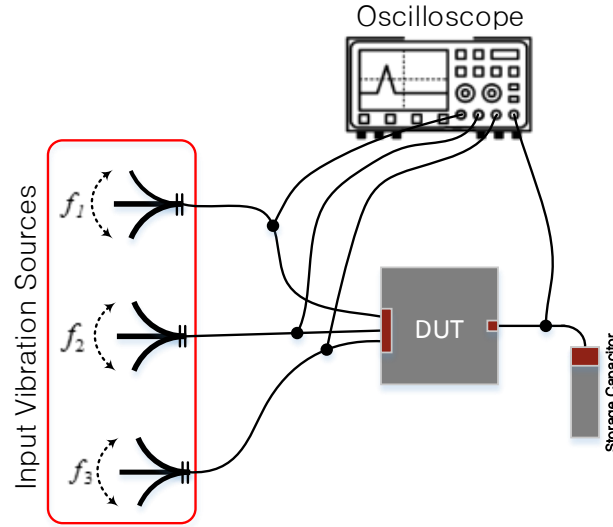


Figure 5.2: Experimental test setup

devices at the peak of their displacements (peak of their terminal voltages). Figure 5.3(a) shows the measured terminal voltage of the 100Hz input vibration source showing a peak to peak voltage of 4.2V. The terminal voltages for both 100Hz and 120Hz inputs are shown in Figure 5.3(b). Using these sources the chip was able to charge a $400\mu F$ capacitor by 770mV in about 5 seconds even with anti-phase input vibrations. The measured charging performance is shown in Figure 5.4 This represents 0.217mJ of extracted energy at a rate of $43.4\mu W$. By sweeping the phase difference between the input sources, the performance of the chip over various input phase differences was determined. This is shown in Figure 5.5. While the power output for vibration sources connected in parallel drops significantly with increasing phase difference, the system maintained fairly constant output power over all vibration phases differences.

The total input power was $80.4\mu W$ giving a measured efficiency of 53.9% which is in close agreement with expected efficiency of 60% obtained from simulation.

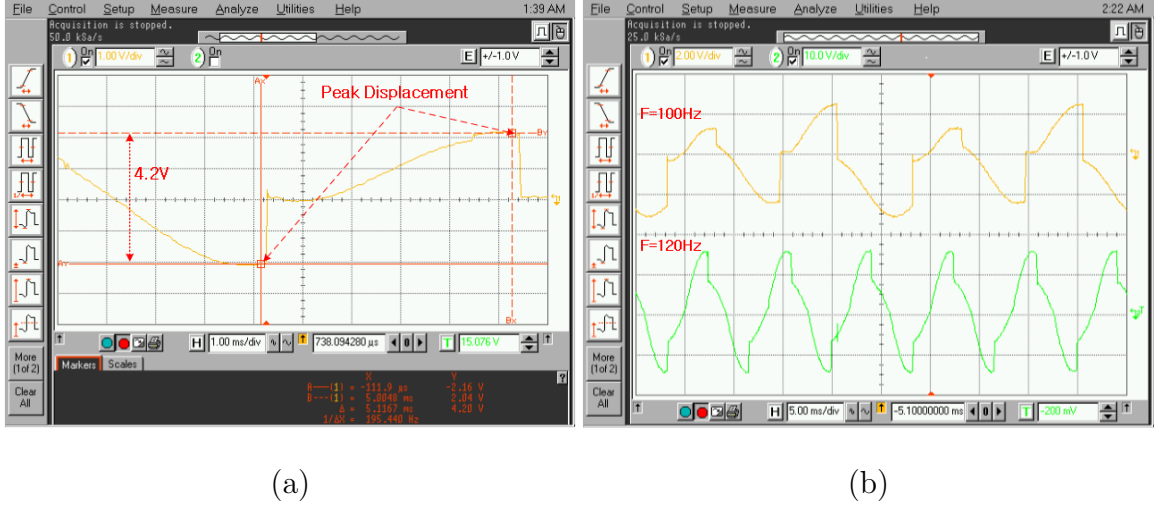


Figure 5.3: Measured waveforms at terminals of vibration sources (a) Single input (b) Two inputs

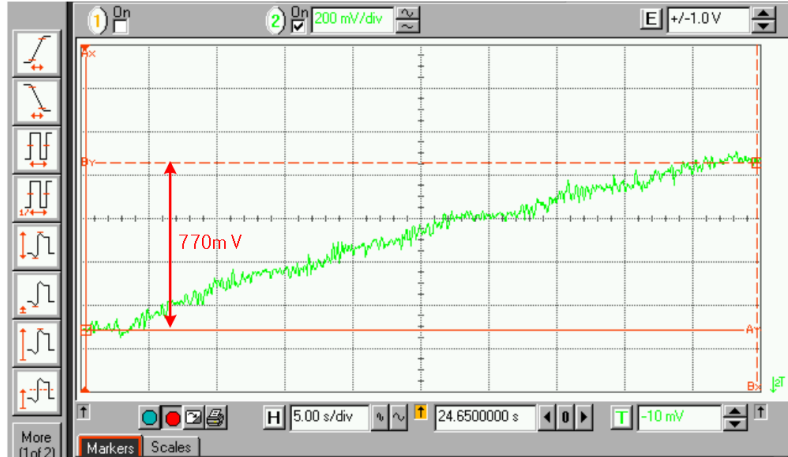


Figure 5.4: Measured charging profile for $400\mu F$ capacitor

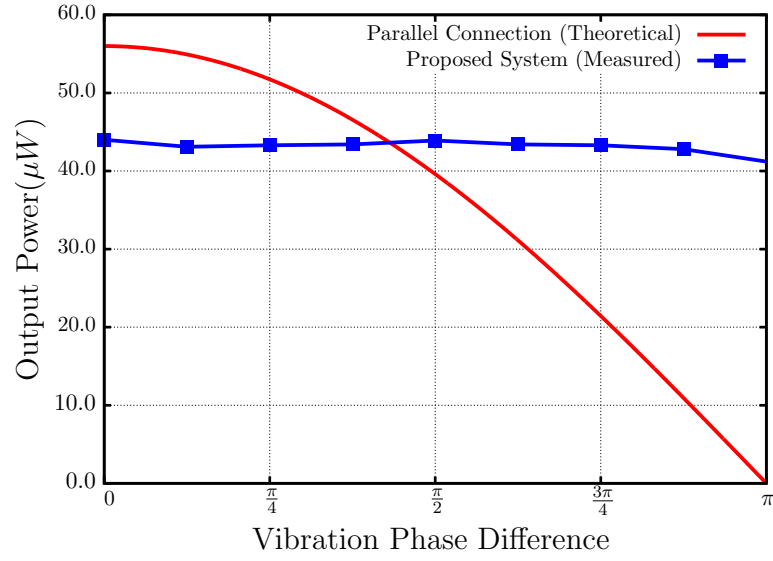


Figure 5.5: Variation of output power with vibration phase difference

Table 5.1: Comparison of results

| Parameter | This Work | [10] | [12] | [8] | [13] | [49] |
|-------------------------------|-------------------------------------|-----------------|--------------------|--------------------|--------------------|--------------------|
| Process | 0.18μm | 2 μm | 0.35 μm | 0.35 μm | 0.35 μm | 0.35 μm |
| Extraction Method | SECE | SECE Injection | SECE | Parallel SSHI | SECE Pile-up | Voltage Doubler |
| Vibration Amplitude (V) | 0.75 | 0.9 | 1 | 2.4 | 0.65** | 1 |
| Output Power(μW) | 60 | 30 | 51 | 32.5 | 87 | 90 |
| No. of Inputs | 3 | 1 | 1 | 1 | 1 | 4 |
| Efficiency | 59.08% | 41.6% | 69.2% | 87%* | 74.9% | 98.3%*** |

*DC-DC converter only

**Increased to $7V_{p-p}$ by energy pile-up

***Rectifier only

The performance of the chip in comparison to the state of the art is summarized in Table 5.1. Most of the previous work is however limited to single inputs, or multiple inputs vibrating synchronously. The only other multiple input harvester in the literature is [49] which was designed for four inputs. The harvester achieves a very high efficiency by using a synchronous rectifier with a very low dropout voltage. The system does not perform MPPT, thereby forgoing any power consumption associated with it. This also contributes to the very high efficiency reported. The voltage doubler topology used however limits the maximum power that the circuit can extract from. The SECE technique used in the proposed architecture can extract 4X more power for vibrations of the same amplitude. Initial energy injection could not be applied for this design due to the limited breakdown voltage of the process. More energy could be harvested if higher voltage processes are used. The harvester compares favorably with the state of the art in terms of efficiency even with three input devices. The harvester has the added advantage of maintaining a high power output independent of vibration phase difference all with a single inductor. The low breakdown voltage of the $0.18\mu m$ process limits the maximum input power of the system. Higher voltage processes could greatly increase efficiency by increasing output power with the same average power consumption ($5.5\mu W$).

6. CONCLUSIONS AND FUTURE WORK

The current push for portable electronic devices and increased wireless connectivity only promises to get stronger, as will the push for increased battery life in these devices. While energy harvesting solutions provide a viable alternative, they are only as effective as their interface circuits will allow. An effective interface circuit should create optimum conditions for power extraction at minimum power cost. This thesis has focused on energy harvesting from piezoelectric transducers. An effective interface circuit has been presented that harvests maximum power from three asynchronously vibrating input sources. The proposed harvester harvests $60\mu W$ of power from three input sources vibrating asynchronously at an efficiency of 60% while consuming about $5.5\mu W$ of power. The system also harvests $1.28\mu J$ from uncorrelated random vibrations, charging a $300\mu F$ capacitor by 240mV in 5 seconds.

Future work could include further mechanical test to investigate the end to end efficiency of the system while harvesting energy from multiple devices. The potential also exists for a fully self sustaining topology in which all rails are internally generated. This would involve the use of an auxiliary rectifier which would charge a storage capacitor to power the circuits at start-up. The main storage capacitor is switched in when it becomes sufficiently charged.

For very low frequency vibrations, many fallow periods still exist in inductor current which could be use to harvest energy from even more devices. This could be investigated further to formally evaluate the limits of the system.

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